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AN ANALYSIS OF ITS USE IN A
PARALLEL INVERTER

NGUYEN VAN

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AN ANALYSIS OF IT'S USE IN A

PARALLEL INVERTER

by

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Lieutenant Commander, Viet-nam Navy

Submitted in partial fulfillment of
the requirements for the degree of

MASTER OF SCIENCE
IN
ELECTRICAL ENGINEERING

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ABSTRACT

The silicon controlled rectifier have been put into use only since 1957. Because of its many advantages over the existing devices such as Thyratrons, magnetic amplifiers, vacuum tubes, power transistors, etc., the SCR has replaced the above devices in many military, industrial as well as commercial applications.

This paper is divided into three chapters. The theory of transistors with particular application to the SCR is discussed briefly in Chapter I.

- An analysis of the parallel inverter SCR is given in Chapter II.

- An experimental circuit design with data and results is given in Chapter III.

The author wishes to express his thanks to the technicians of the U. S. Naval Postgraduate School Electrical Engineering and photographic laboratories for their assistance in constructing the circuit and photographing different results of the experimental set up.

He especially wishes to extend his appreciation and gratitude to Professor William Conley Smith of the Department of Electrical Engineering for his assistance and encouragement in the completion of the paper.

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THE SILICON CONTROLLED RECTIFIER OPERATION

I.1 Introduction.

The Silicon controlled Rectifier (SCR) is a P-N-P-N semi-conductor device with three external leads: one is at the end P region which is called the anode, another is at the end N region called the cathode and the last one is at the P region in the center called the gate. (See Figure 1.1 below).
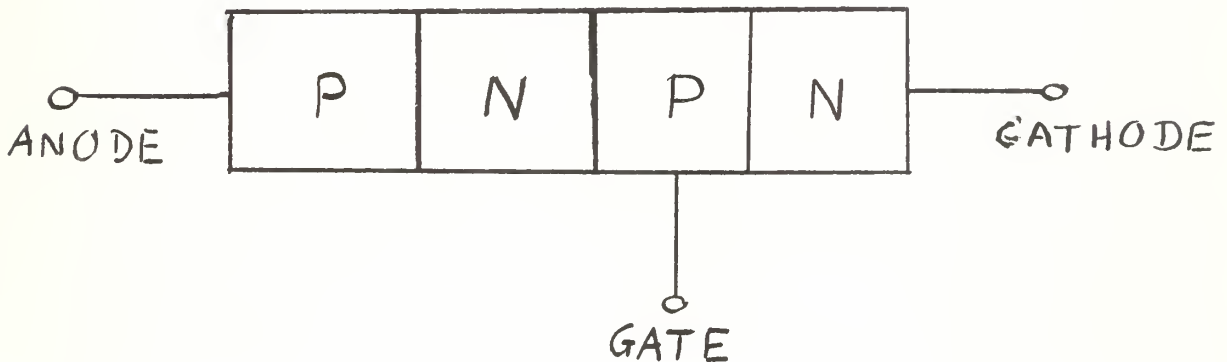
Fig. 1.1 An P-N-P-N controlled rectifier

The device has three regions of operation:

The device is "off" when there is a reverse voltage, i.e., when its cathode is made more positive than its anode. "Off" condition of the SCR means that there is very little current flowing through, i.e., the SCR is not conducting.

The device is still in the "off" condition when a forward voltage smaller than its breakover forward voltage, is applied at its terminals (anode and cathode).

However when a forward voltage is applied at its terminals and a small positive current pulse is injected into the gate, then the SCR is switched on, and current flow from anode to cathode is limited only by the external impedance.

Once the device has switched "on", i. e., to the low impedance state, the trigger (current pulse from the gate) may be removed and the device will remain "on".

To turn "off" the SCR, we have to reduce the anode to cathode current by applying a reverse voltage to its terminals, or in low power SCR's, by applying a negative current pulse from the gate to cathode terminals.

As the SCR is a P-N-P-N semi-conductor device, in order to understand its operation, the best way is to investigate the P-N junction, the N-P-N transistor and finally the P-N-P-N controlled rectifier devices.

I.2   The P-N Junction.

A P-N junction is made by growing a single semi-conductor crystal part of which is N-type and part P-type.

The N-type is a crystal lattice semi-conductor when doped with a donnor impurity such as elements in the fifth column of the periodic table, like arsenic, antimony and phosphorus; they are called donnor impurities because they can donate an extra electron to the crystal.

On the other hand the P-type is a crystal lattice semi-conductor when doped with an acceptor impurity like aluminum, gallium or indium; they are called acceptors because they can accept free electrons from the semi-conductor crystal.

The boundary inside the crystal between the P- and N- regions is called a P-N junction. A P-N junction must be fabricated as a single crystal in order for the junction to have interesting electrical properties.

In a P-N junction at thermal equilibrium, when the temperature is high enough, the excess electrons from the donnor impurity atoms are in conduction band and the excess holes from the acceptor impurity atoms are in the valence band. (See Fig. 1.2).

Figure 1.2 shows the crystals before contact. Since they are identical except for impurity content, the bands occur at the same energies in each crystal and the Fermi-levels /1/ are not aligned.

When the crystals are joined, electrons spill over from the higher level of the N side to the P side and holes spill the other way. (See Fig. 1.3).

The diffusion of electrons and holes stops when the Fermi-levels are lined up. Figure 1.4 represents the equilibrium situation when there is no bias voltage across the device, i.e., there is no net current flowing across the junction.
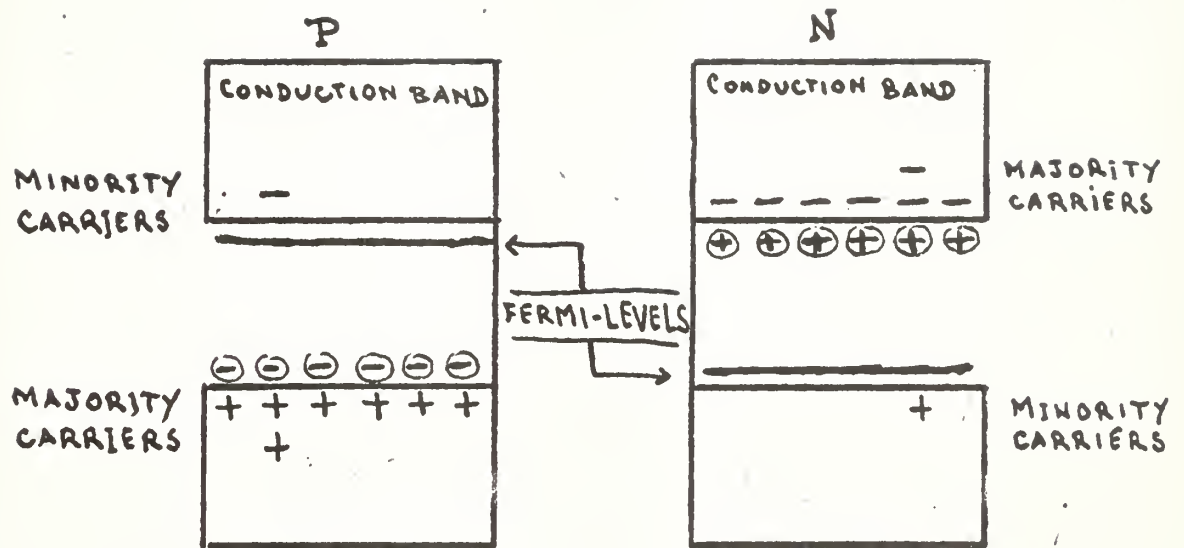
Fig. 1-2 P-N junction before contact
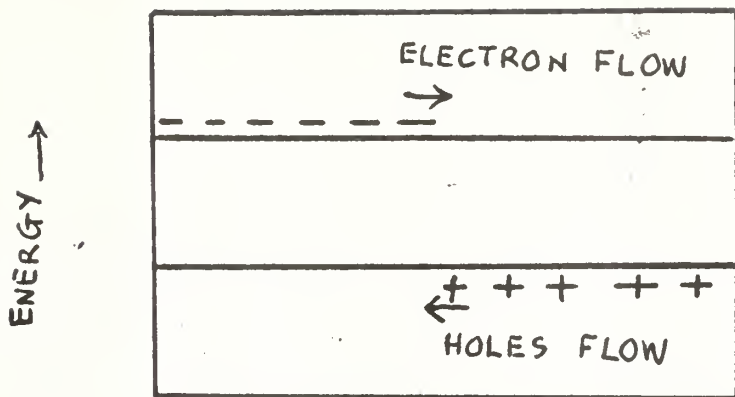
Fig. 1-3 P-N junction immediately following
contact
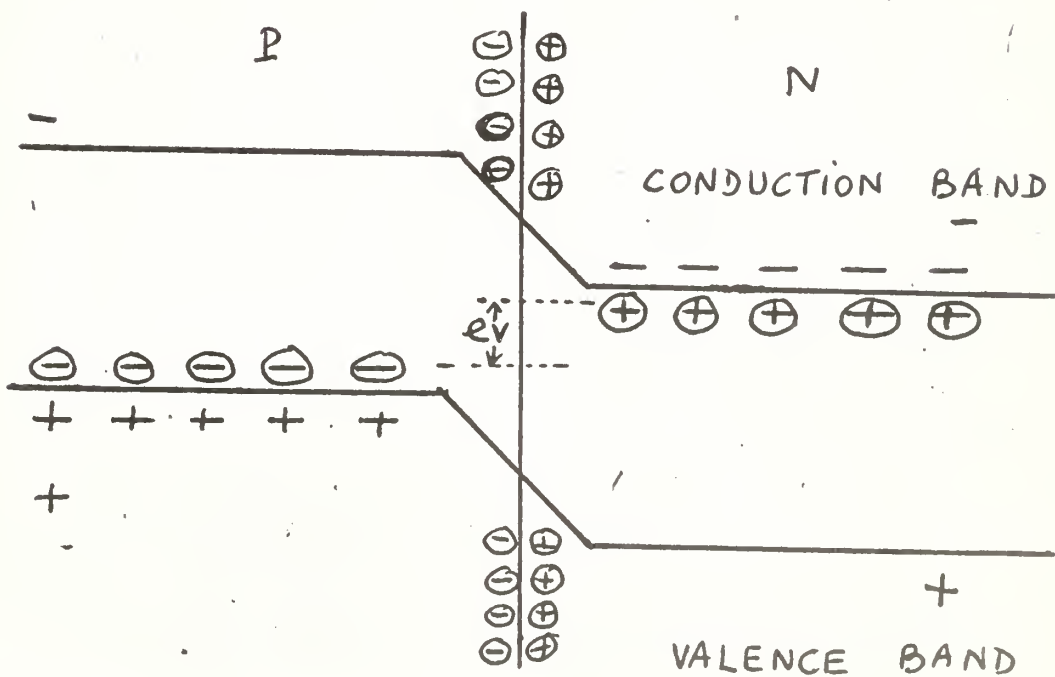
1-3bis P-N junction reversed biased
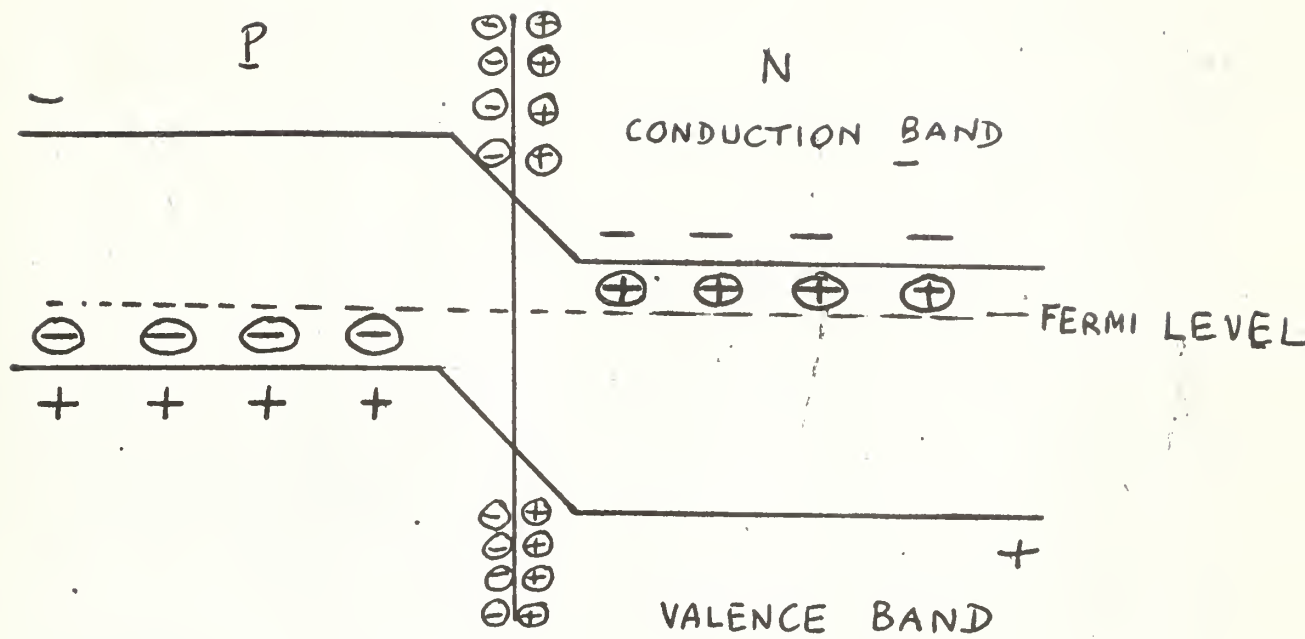
Fig. 1-4   P-N junction, no bias voltage
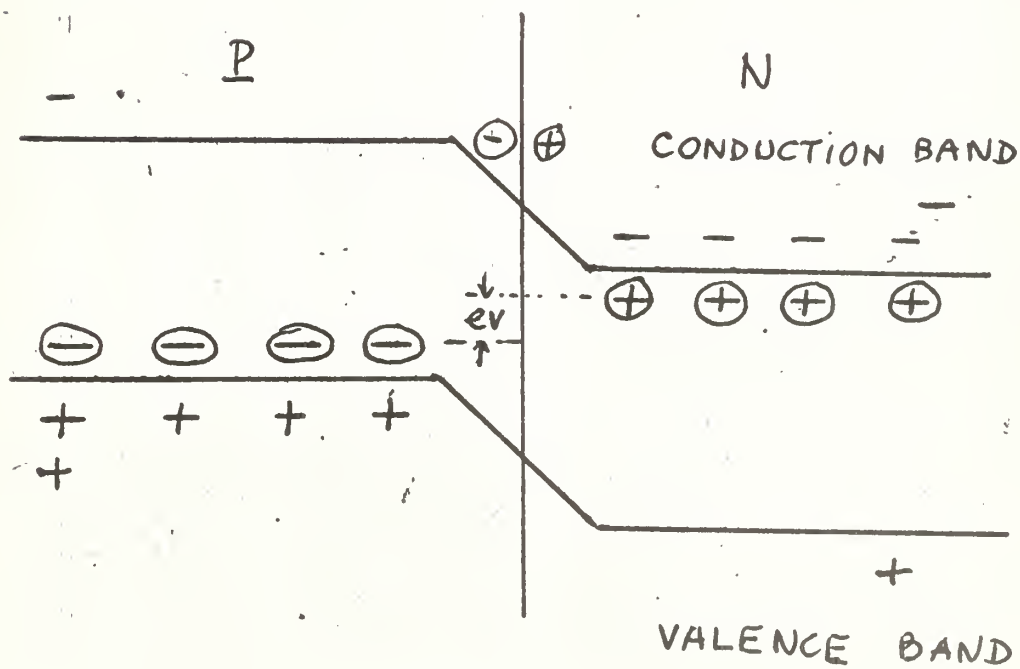
Fig. 1-4 bis   P-N junction, forwarded biased

The excess positive charges that accumulate on the N-side and the negative charges that accumulate on the P-side reside on the surface of the crystals and on both sides of the junction. The double layer of charge at the junction consists of negative acceptor ions on the P-side and positive donnors on the N-side. This double charge layer region is called the depletion layer and is responsible for the depletion layer capacitance which can be approximated by the following formula /1/:

$$C_{d\ell} = \frac{k \, \epsilon_o \, A}{d_p + d_n} \qquad (1\text{-}1)$$

where $C_{d\ell}$: depletion layer capacitance in farads

    k : relative dielectric constant of the semi-conductor in farads/meters

    ϵ_o : dielectric constant for free space in farads/meters.

    A : junction area in square meters

    d_p, d_n: thickness of the depletion layer on the P and N-sides in meters.

This capacitance is an important factor in the operation of the solid-state parameter amplifier and can be a limiting factor in the high frequency performance of a transistor.

The total width of the depletion layer $d_p + d_n$, in the case of an abrupt junction is:

$$d_p + d_n = \left[\frac{2 k \epsilon_o}{q} \left(\frac{1}{N_p} + \frac{1}{N_n} \right) \right]^{\frac{1}{2}} \left(V_r \right)^{\frac{1}{2}} \qquad (1\text{-}2)$$

where V_r is the potential across the depletion layer, N_p, N_n are the density of free holes and free electrons in the valence band and

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q is the charge of an electron in coulomb.

Equation (1-2) shows that the width of the depletion layer increases as the junction becomes more reverse biased (V_{rc} increased).

If we apply a voltage across the terminals of the P-N device, the energy level on the two sides will all shift relative to one another by the amount $\mathcal{C}V$. (See Fig.1-3bis).The direction of the shift depends on the polarity of the applied voltage. If the device is forward biased, i.e., when the P-side is made positive and the N-side negative, the applied voltage will reduce the excess negative charge on the P-side, raise the potential and therefore lower the potential energy of electrons. At the same time the applied voltage reduces the excess positive charge in the N-side, the potential is lowered and the potential energy is raised, the Fermi-level on the N-side is raised above the Fermi-level on the P-side, therefore electrons can flow from the N-side to the P-side. This flow of electrons will make possible recombination with the majority carriers, holes, in the P-side. The recombination component of current is given by /2/; See Fig. 1-5:

$$ J = J_n + J_p = q \left(\frac{D_h\, P_n}{L_p} + \frac{D_e\, N_p}{L_n} \right) \left(e^{\frac{-qV}{kT}} - 1 \right) \tag{1-3} $$

where J : total junction current density in amp/cm^2/

J_p : current density due to holes in amp/cm^2/

J_n: current density due to electrons in amp/cm^2/

q : charge of an electron or hole in coulomb

D_h : diffusion constant for holes in cm^2/sec

D_e: diffusion constant for electrons in cm^2/sec

P_n: holes density in N-region in $1/cm^3$/

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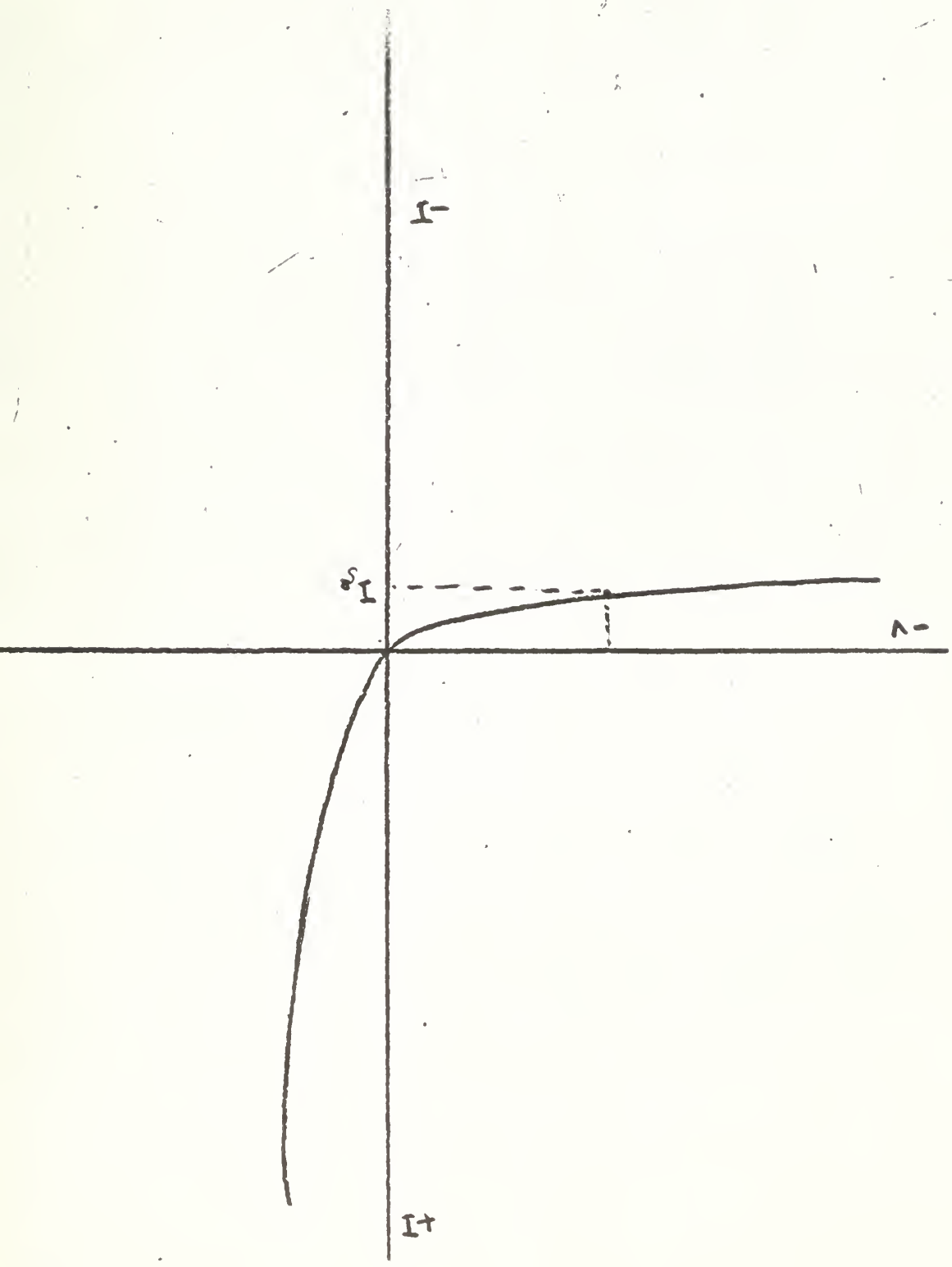
N_P : electrons density in P-region in $1/cm^3/$

L_n : diffusion length for electrons in cm

L_P : diffusion length for holes in cm

k : Boltzman constant in $\dfrac{joule}{molecule\ °K}$

T : absolute temperature in degree Kelvin

The first part of equation (1-3) is a constant for a given device and is called the reserve saturation current density, I_s . Equation (1-3) becomes:

$$ I_t = I_s \left(e^{-\frac{qV}{kT}} - 1 \right) \tag{1-4}$$

where I_t : total junction current in amperes

              I_s : reverse saturation current in amperes

              V : applied voltage across the P-N device, positive for forward bias and negative for reverse bias voltage.

If applied voltage is connected as reverse biasing, that is, positive at the N-side and negative at the P-side, this will raise the energy levels on the P-side and lower them on the N-side. However, since there are very few electrons in the conduction band on the P-side which are available to spill over, the electron current is very small. Also there are very few holes, spilling over from the N-side to the P-side.

I.3 The N-P-N Transistor.

The N-P-N transistor is a solid-state device that contains two P-N junctions in a single crystal structure as shown in Figure 1-6 below:
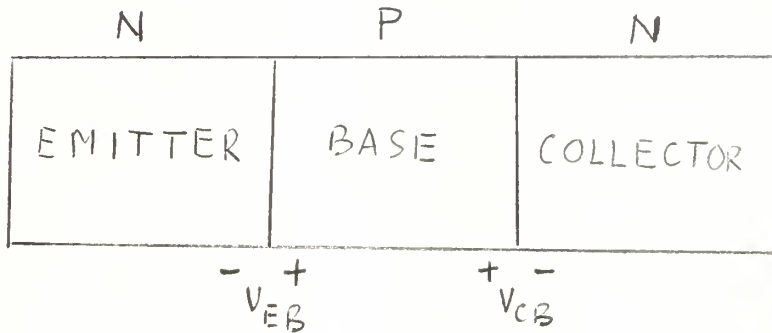
Fig. 1-6 N-P-N Transistor.

The ends of a transistor sandwich known as the emitter and collector, are heavily doped with impurity atoms. The middle of the sandwich, known as the base, is thin and contains a relatively small concentration of impurity atoms. In the N-P-N type transistor, most of the current is carried by electrons, and in the P-N-P type transistor, most of the current is carried by holes.

In normal operation of a transistor, the emitter base junction is usually forward biased and the collector junction is reverse biased.

Figure 1-7 shows an N-P-N transistor with no bias voltage. With no bias voltage, the sum of the recombination current and the thermal current across each junction is equal to zero.

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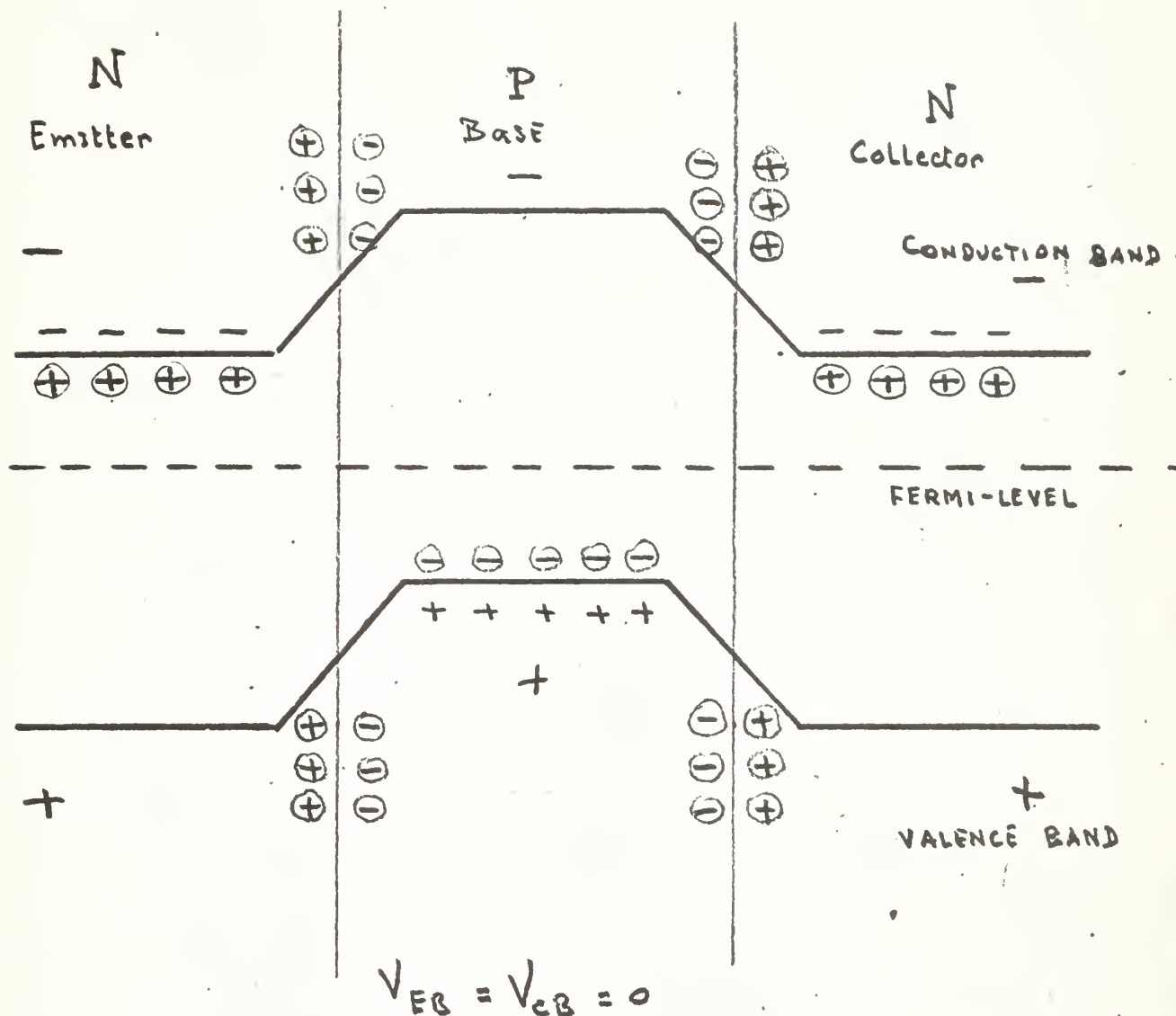
Fig. 1-7 N-P-N transistor, no bias voltage

Figure 1-8 shows an N-P-N transistor with normal bias voltage.

As previously stated in the normal operation the junction between the emitter and base region is forward biased ($V_{EB} > 0$) and that between the collector and base is reverse biased ($V_{CB} < 0$) as shown in Fig. 1-6, conduction electrons spill over from the N-type emitter into the P-type base region. The equations for the currents at each junction are as follows /3/, /4/:

$$I_c = I_{cs} \left(e^{q V_{CB}/kT} - 1 \right) - \alpha_n I_{es} \left(e^{q V_{EB}/kT} - 1 \right) \qquad (1-5)$$

$$I_e = I_{es} \left(e^{q V_{EB}/kT} - 1 \right) - \alpha_i I_{es} \left(e^{q V_{CB}/kT} - 1 \right) \qquad (1-6)$$

where I_{es}, I_{cs} : are the emitter and collector saturation current
similar to in equation (1-4).

α_n : the normal current gain

α_i : the inverted current gain (with the emitter and collector interchanged)

V_{CB}, V_{EB} are defined in Fig. (1-6)

Equations (1-5) and (1-6) above show that the current flow across each junction is composed of two parts, one due to majority carrier flow due to the forward bias voltage and the other due to the portion of the injected current collected at the collector junction.

Equations (1-5) and (1-6) can be modified as follows /3/:

$$I_e = I_{eo} \left(e^{q V_{EB}/kT} - 1 \right) - \alpha_i I_c \qquad (1-7)$$

$$I_c = I_{co} \left(e^{q V_{CB}/kT} - 1 \right) - \alpha_n I_e \qquad (1-8)$$

Where I_{eo} and I_{co} are defined as follows:

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N
Emitter

P
Base

N
Collector

Fermi-level

$V_{EB} > 0$ $V_{CB} > 0$
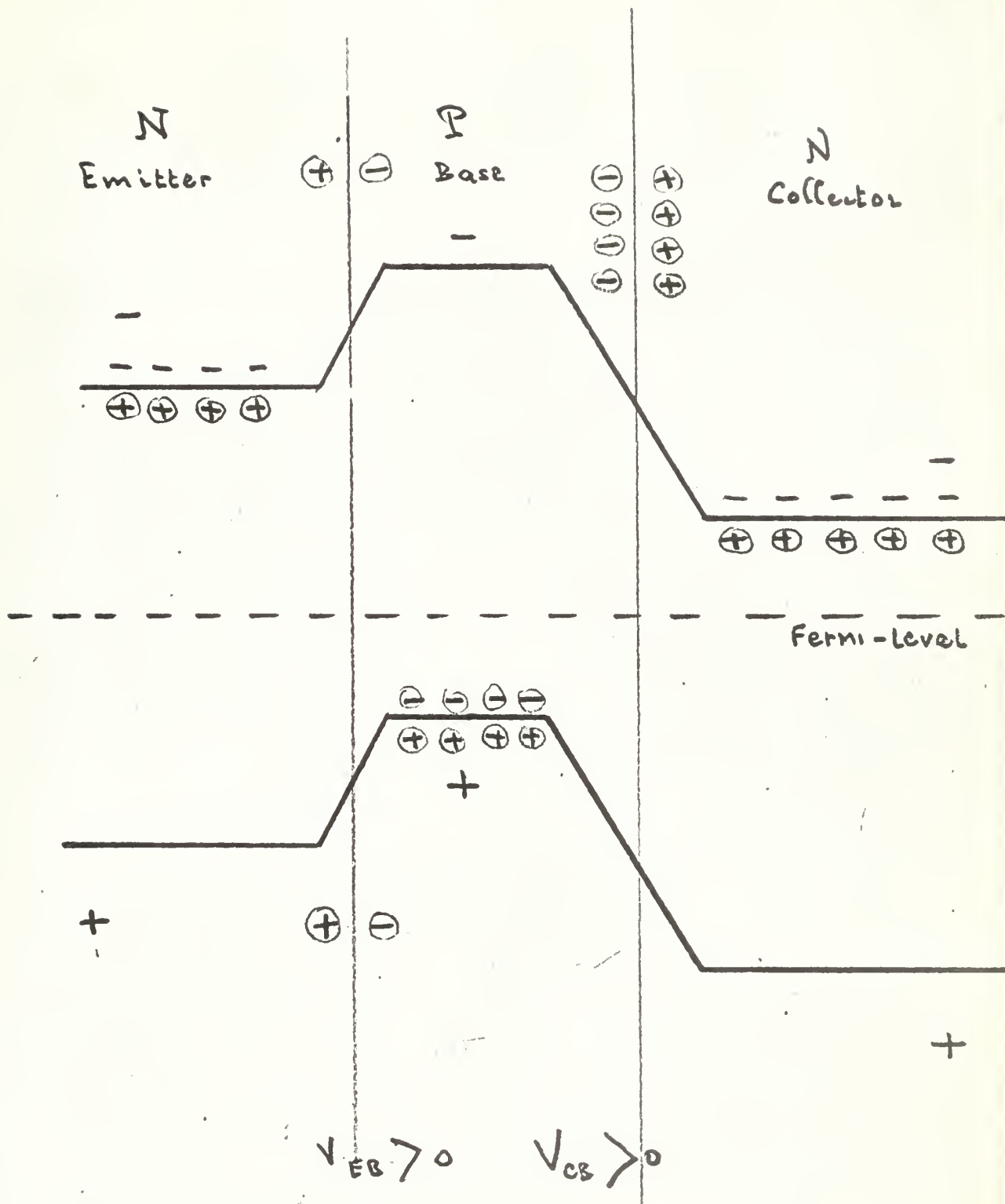
Fig. 1-8 N-P-N transistor, normal bias voltage

$$I_{eo} = (1 - \alpha_n \alpha_i) I_{cs} \tag{1-9}$$

$$I_{co} = (1 - \alpha_n \alpha_i) I_{cs} \tag{1-10}$$

It can also be shown that, for low level operation /4/,

$$\alpha_n I_{es} = \alpha_i I_{cs} \tag{1-11}$$

The above developments are solved for a common base transistor where the base terminal is common to both the input and output circuits as shown on Figure 1-6.

When the emitter is common to both the input and output as shown on Figure 1-9, the Equations (1-5) through (1-10) are modified as follows:

$$I_c = \alpha_n I_{es} \left(e^{q V_{EB}/kT} - 1 \right) - I_{cs} \left(e^{q V_{cb}/kT} - 1 \right) \tag{1-12}$$

$$I_e = (1 - \alpha_n) I_{es} \left(e^{q V_{EB}/kT} - 1 \right) + (1 - \alpha_i) I_{cs} \left(e^{q V_{cb}/kT} - 1 \right) \tag{1-13}$$

where I_c is the current flowing into the collector and I_e is the current flowing into the base.

There are three normal regions of operation for all transistors.

Region I is called the cut-off region because both junctions are reverse biased, that is V_{cB} and V_{EB} are negative.

Region II is called linear region of operation because the emitter to base junction is forward biased, $V_{EB} > 0$, while the collector to base junction is reverse biased, $V_{cB} < 0$.

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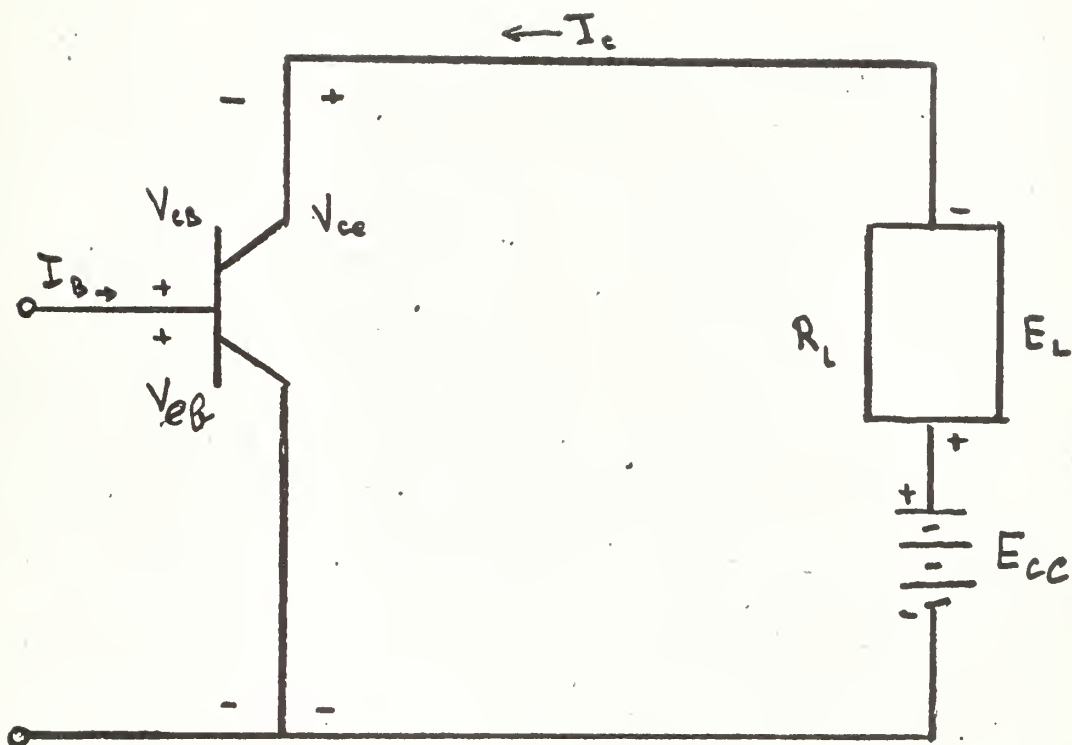
Fig. 1-9 Common emitter N-P-N transistor switch

Region III is called the saturated region because both junctions are forwarded biased, V_{CB} and V_{EB} are both positive.

The current flowing from collector to emitter in region I is small, the equation of that current can be obtained by substituting $V_{CB} < 0$ and $V_{EB} < 0$ into equations (1-12 and 1-13) so that the exponential terms can be neglected, and remembering that :

$$\alpha'_m I_{es} = \alpha_i I_{cs} \qquad \text{(from Equation 1-11)}$$

then: /3/
$$I_c = (1 - \alpha_i) I_{cs} \qquad (1-14)$$

Equation (1-14) shows that the collector current is very small, under these conditions, most of the collector bias battery voltage V_{CC} appears on the transistor from collector to emitter.

In region II, $V_{EB} > 0$, $V_{CB} < 0$, substituting these conditions into equations (1-12) and (1-13), we obtain the following expression for the collector current: /3/:

$$I_c = \frac{\alpha_m I_b + I_{co}}{1 - \alpha_m} \qquad (1-15)$$

Neglecting the I_{co} term, the collector current is proportional to the base current and hence the load voltage ($I_c R_L$) is proportional to the base current. This is why region II is called the linear region.

Now let
$$\beta = \frac{\alpha_m}{1 - \alpha_m} \qquad (1-16)$$

We see that when $\alpha_m = .975$ for example, $\beta = 39$, this means that the base current need be only 2.5 % of the collector current. β is called the grounded emitter current gain.

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In region III, both V_{EB} and V_{CB} are positive. This gives the following expression for V_{CE} , from equations (1-12) and (1-13) /3/:

$$V_{CE} = \frac{kT}{q}(1 - \alpha_i')$$

(1-17)

Equation (1-17) assumes that the base current is sufficient to cause the transistor to be well into the saturated region. This means that almost the entire collector bias voltage (V_{CC}) appears across the load resistor. The collector current then is limited only by the load resistance.

1.4 The P-N-P-N Controlled Rectifier.

The current and voltage equations for a P-N-P-N controlled recifier
can be determined by a similar method used for the P-N junction and N-P-N
transistor. The current and voltage at different junctions are defined ac-
cording to Fig. I-10:

The equations for the junction currents are /5/, /6/, and /7/:

$$I_1 = I_{S1}\left(e^{\beta V_1} - 1\right) - \alpha_{1i} I_{S2}\left(e^{\beta V_2} - 1\right) \tag{1-18}$$

$$I_2 = \alpha_{1n} I_{S1}\left(e^{\beta V_1} - 1\right) - I_{S2}\left(e^{\beta V_2} - 1\right) - \alpha_{2n} I_{S3}\left(e^{\beta V_3} - 1\right) \tag{1-19}$$

$$I_3 = -\alpha_{2i} I_{S2}\left(e^{\beta V_2} - 1\right) + I_{S3}\left(e^{\beta V_3} - 1\right) \tag{1-20}$$

where:

α_{1n} : normal alpha with junction one emitting and
junction two collecting.

α_{1i} : inverted alpha with junction two emitting and
junction one collecting.

α_{2n} : normal alpha with junction three emitting and
junction two collecting.

α_{2i}' : inverted alpha with junction two emitting and
junction three collecting.

I_{S1} , I_{S2} , I_{S3} are the saturation currents for junctions one, two
and three in amperes

Equation (1-18) has four terms. The first term is due to the majority

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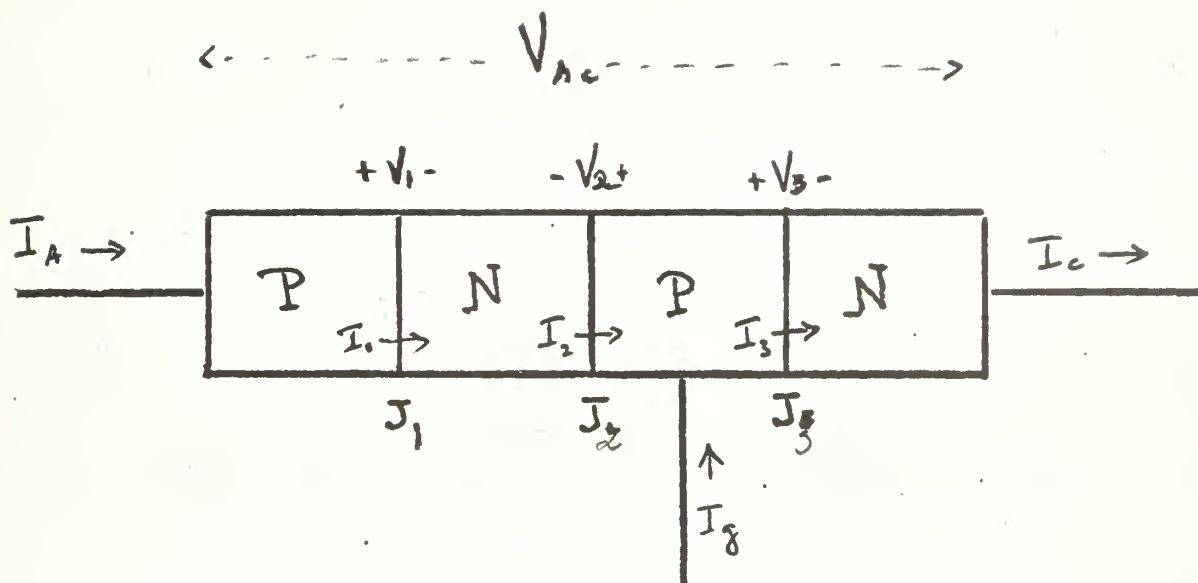
Fig. 1-10 Currents and Voltages in a P-N-P-N
Controlled rectifier

carriers, holes, crossing junction one, the second term is due to the minority carriers crossing junction one, the third term is due to the holes injected at junction two diffusing through the N-region and crossing junction one, the last term is due to the minority carriers from junction two diffusing through the N-region and crossing junction one. The current flowing through junction three also has four terms as shown on equation (1-20), but the current flowing through junction two has six terms because of current flow from both junctions one and three.

The junction voltage can be solved in terms of the junction currents given by equations (1-18), (1-19) and (1-20) to give /5/, /6/ and /7/:

$$V_1 = \frac{1}{\beta} \ln \left[\frac{I_1(1-\alpha_{2n}\alpha_{2i}) - \alpha_{1i} I_2 + \alpha_{1i} \alpha_{2n} I_3}{I_{S1}(1-\alpha_{1n}\alpha_{1i} - \alpha_{2n}\alpha_{2i}} + 1 \right] \qquad (1\text{-}21)$$

$$V_2 = \frac{1}{\beta} \ln \left[\frac{\alpha_{1n} I_1 - I_2 + \alpha_{2n} I_3}{I_{S2}(1-\alpha_{1n}\alpha_{1i} - \alpha_{2n}\alpha_{2i})} + 1 \right] \qquad (1\text{-}22)$$

$$V_3 = \frac{1}{\beta} \ln \left[\frac{\alpha_{1n}\alpha_{2i} I_1 - \alpha_{2i} I_2 + I_3(1-\alpha_{1n}\alpha_{1i})}{I_{S3}(1-\alpha_{1n}\alpha_{1i} - \alpha_{2n}\alpha_{2i})} + 1 \right] \qquad (1\text{-}23)$$

Fig. I-10 enables us to write:

$$I_a = I_1 = I_2 \qquad (1\text{-}24)$$

$$I_c = I_3 \qquad (1\text{-}25)$$

$$I_g = I_c - I_a \qquad (1\text{-}26)$$

where I_a = anode current in amps

$\quad\quad I_c$ = cathode current in amps

$\quad\quad I_g$ = gate current in amps

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Because of the complexity of the equations (1-18) through (1-23) the volt-ampere characteristics of the SCR will be divided into three regions of operation: I, II and III.

I.4a P-N-P-N Controlled Rectifier, Region I

Region I or the reverse blocking state of the SCR occurs when its anode is made negative and cathode positive, thus $V_{AC} < 0$.

From Figure I-10 we can see that in Region I, junctions one and three are reverse biased, and junction two is forward biased. From our previous investigation on the P-N junction, we can conclude that the device will allow a very small leakage current flowing from the cathode to anode.

Now if, $V_1 \gg \beta$, as in the reverse biasing $V_1 < 0$, then $e^{\beta V_1} - 1 \simeq -1$, if $V_2 \gg \beta$, then $e^{\beta V_2} - 1 \simeq e^{\beta V_2}$ as $V_2 > 0$ (forward biasing)

Similarly $e^{\beta V_3} - 1 \simeq -1$

Now substituting the above approximated values into equations (1-18), (1-19) and (1-20) at the same time, using equations (1-24), (1-25) and (1-26), we obtain:

$$I_a \quad = -\left[I_{s_1} \left(\frac{1 - \alpha_{1i} \alpha_{1n} - \alpha_{2i} \alpha_{2n}}{1 - \alpha_{1i} - \alpha_{2m} \alpha_{2i} - \alpha_{2n} \alpha_{1i}} \right) + I_g \left(\alpha_{2n} - \alpha_{1n} \right) \right] \quad (1-27)$$

Equation (1-27) shows that in region I, the anode current is negative, it is proportional to the saturation current across junction one (equal to a fraction of it), this current also depends on the value of the gate current. It increases with the gate current which gives the increasing temperature at the junction and can cause thermal runaway. The manufacturer specifies

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limit the gate current during the reverse blocking state of the SCR. The
amount of the reverse leakage current I_a , region I, is about 10 mil-
liamperes in present devices /8/.

Figure 1-11 shows the energy diagram of the SCR in region I.

I.4b P-N-P-N Controlled Rectifier, Region II.

Region II or the forward blocking state of the SCR occurs when its
anode is made positive and its cathode negative. From Fig. I-10 we see
that in region II, junctions one and three are forward biased, and junc-
tion 2 is reverse biased. Again because of the reverse bias of junction
two, the device will pass little current. Considering for the moment that
there is no gate current, if we increase the applied voltage from anode to
cathode, the accelerating voltage for minority carriers crossing over junc-
tion two will increase, so also will the width of the depletion layer at
junction two (See Equation (1-2)).

As the minority carriers are accelerated across junction two they col-
lide with the fixed atoms of the crystal so that under high enough acceler-
ating voltage, secondary emission of minority carriers might occur, thus in-
creasing the number of majority carriers in order to keep the balance of
charge. Increasing the number of majority carriers crossing junction two is
equivalent to increasing the alpha. Thus, further increase of applied volt-
age can result in an avalanche break down of the junction, the device is then
switched from the forward blockingstate, region II, to the high conduction
state, region III, in which the anode to cathode current is limited only by
external impedance. The value of the applied voltage at which avalanche
breakdown occurs is called the forward breakover voltage which is generally
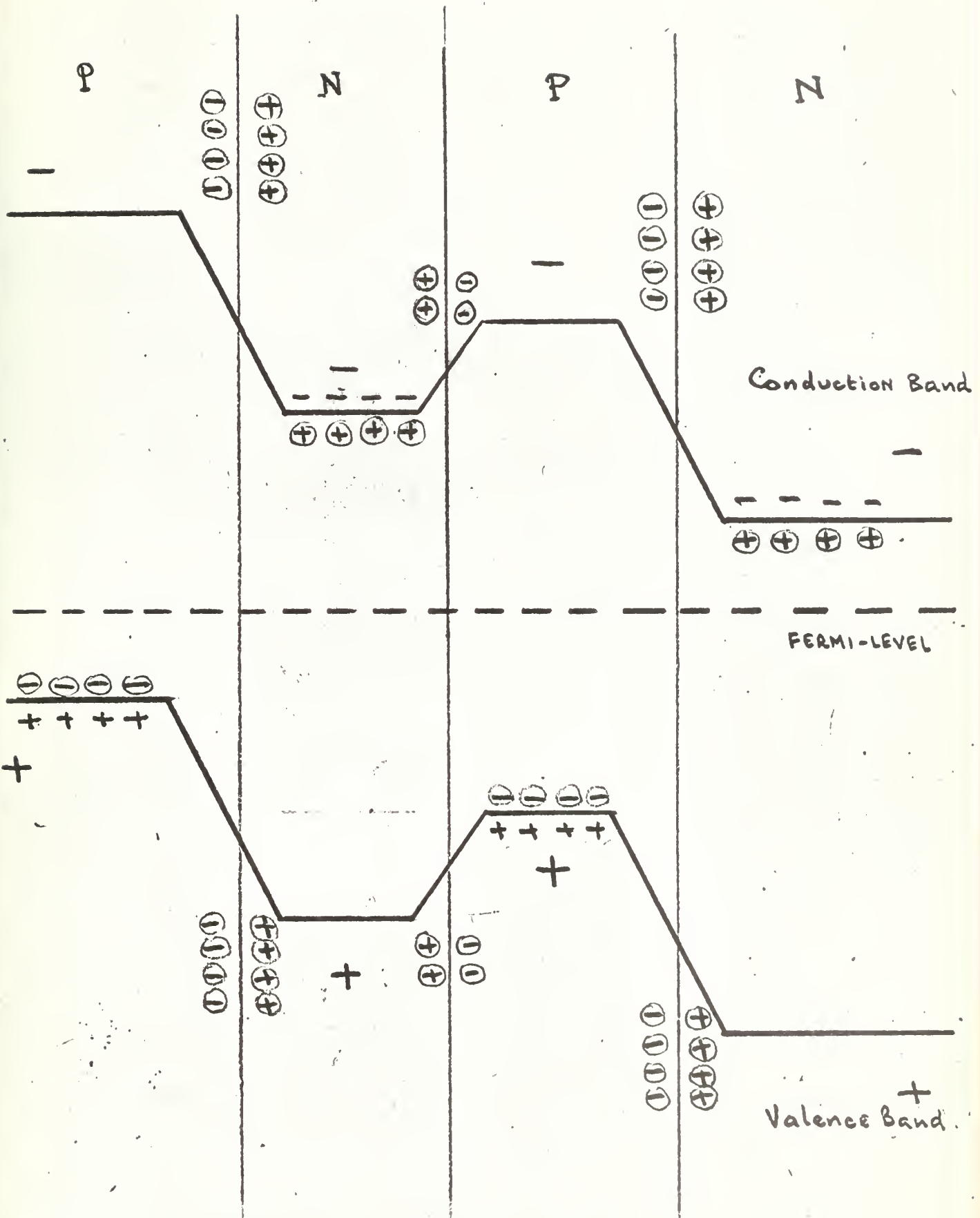equal or slightly greater than the reverse avalanche breakdown voltage.

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Fig. 1-11 P-N-P-N controlled rectifier,
Region I

The gate lead of the SCR allows the injection of minority carriers into the gate, independent of the value of the positive anode to cathode voltage, this is the very practical way to switch the SCR from region II to region III, i.e., by triggering pulse current into the gate.

The time required to switch from region II to region III, the "turn-on" time, is about 1 to 3 microseconds for actual SCR.

As before, assume $V_1 \gg \beta$, $V_2 \gg \beta$ and $V_3 \gg \beta$, as $V_1 > 0$

$V_3 > 0$, and $V_2 < 0$ so that: $e^{\beta V_1} - 1 \simeq e^{\beta V_1}$, $e^{\beta V_2} - 1 \simeq -1$,
$e^{\beta V_3} - 1 \simeq e^{\beta V_3}$

With these assumptions, equations (1-18) through (1-26) can be used to solve for the anode current to give:

$$I_{a, region\ \Xi} = I_{S2} \left(\frac{1 - \alpha_{1n}\alpha_{1i} - \alpha_{2n}\alpha_{2i}}{1 - \alpha_{1n} - \alpha_{2n}} \right) + I_g \left(\frac{\alpha_{2n}}{1 - \alpha_{1n} - \alpha_{2n}} \right) \qquad (1-28)$$

From the above equation, we can see that the anode current in region II has a positive value which is equal to a fraction of the saturation current of junction two, I_{S2} , it also depends on the value of the gate current, and increases with it. The value of the forward leakage current is in the order of 10 milliamperes in actual SCR.

The energy diagram of the SCR in region II is shown on Fig. I-12.

I.4c   P-N-P-N Controlled Rectifier Region III.

In this region all three junctions are forward biased, so that the anode current is limited only by external impedance.

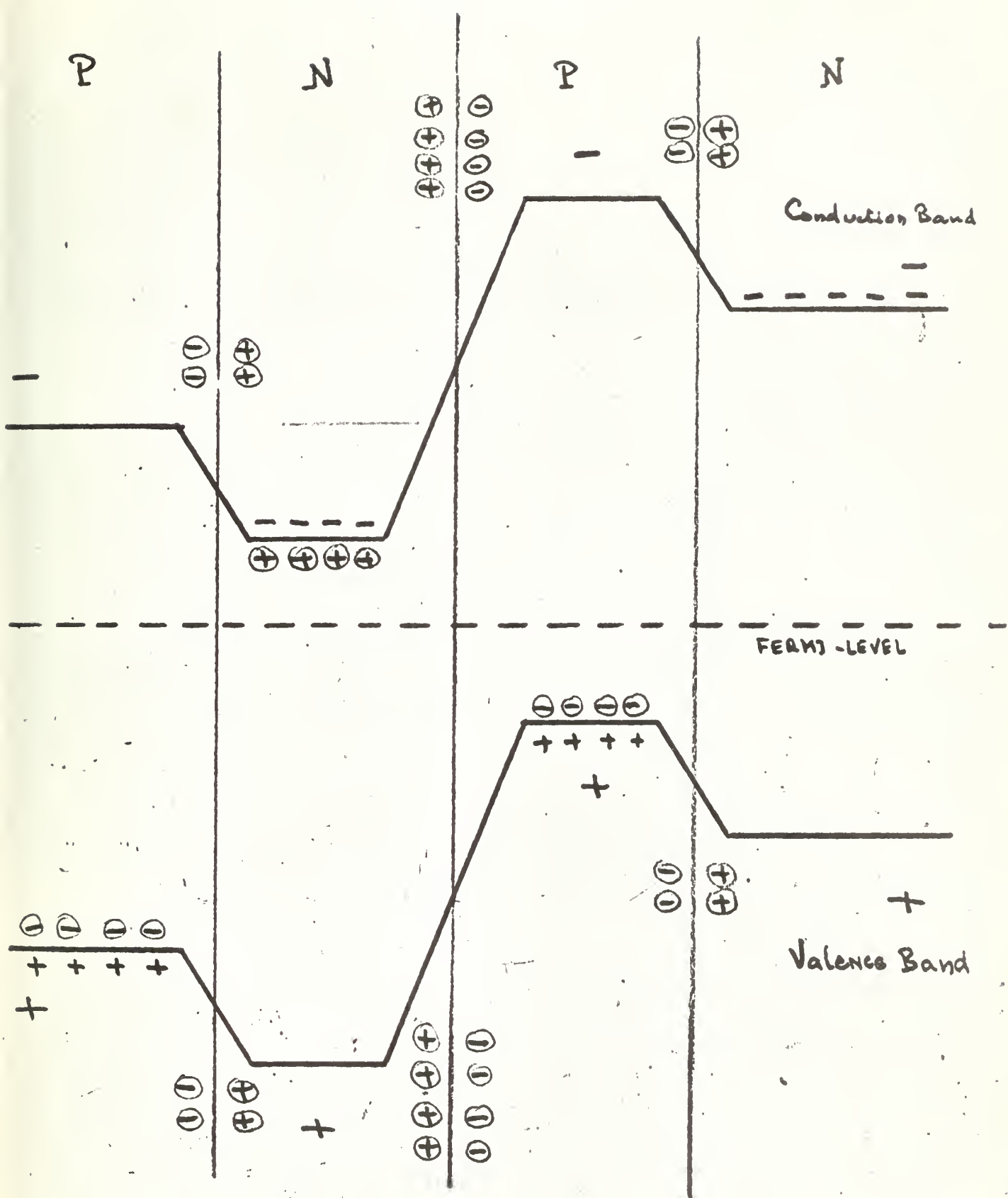Again assuming $V_1 \gg \beta$, $V_2 \gg \beta$, $V_3 \gg \beta$, now V_1 , V_2 and V_3 are all positive so that:

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Fig. 1-12 P-N-P-N controlled rectifier,
Region II

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$$e^{\beta V_1} - 1 \simeq e^{\beta V_1}, \quad e^{\beta V_2} - 1 \simeq e^{\beta V_2}, \quad e^{\beta V_3} - 1 \simeq e^{\beta V_3}$$

With these assumptions made, the voltage across the SCR, V_{AC}, is equal to /5/:

$$V_{AC} = \frac{1}{\beta} Ln \frac{I_{S2} I_a}{I_{S1} I_{S3}} \left[\frac{(1 + \alpha_{1i} \alpha_{2n} - \alpha_{2n} \alpha_{2i})(1 + \alpha_{1n} \alpha_{2i} - \alpha_{1i} \alpha_{1n} - \alpha_{2i})}{(\alpha_{1n} + \alpha_{2r} - 1)(1 - \alpha_{2n} \alpha_{2i} - \alpha_{1n} \alpha_{1i})} \right] \quad (1-29)$$

If $\alpha_{1n} + \alpha_{2n} > 1$, (1-29) can be simplified as follows /5/:

$$V_{AC} = \frac{1}{\beta} Ln \frac{I_{S2} I_a}{I_{S1} I_{S3}} \left(\frac{1}{\alpha_{1n} + \alpha_{2n} - 1} \right) \quad (1-30)$$

If $I_{S1} = I_{S2} = I_{S3}$, then (1-29) can be simplified further as follows:

$$V_{AC} = \frac{1}{\beta} Ln \frac{I_a}{I_S} \left(\frac{1}{\alpha_{1n} + \alpha_{2n} - 1} \right) \quad (1-31)$$

Equation (1-31) can be compared with equation (1-4) of a single forward biased rectifier after we put it in a more simple form:

$$V_{AC} = \frac{1}{\beta} Ln \frac{I_a}{I_S} \quad (1-32)$$

From the above equation, we can see that the voltage drop across the SCR when it conducts, is proportional to the natural log of the anode current, which increases only slightly for a large increase of anode current. The energy diagram of the SCR in region III is shown in Fig. 1-13.

As previously stated, once the SCR is in the "on" condition, it does not need the gate current anymore to keep it "on". To switch the SCR back to its blocking state, we can use one of the following methods:

a) By reducing the anode current to a value below its holding current. The value of the holding current is determined as the condition
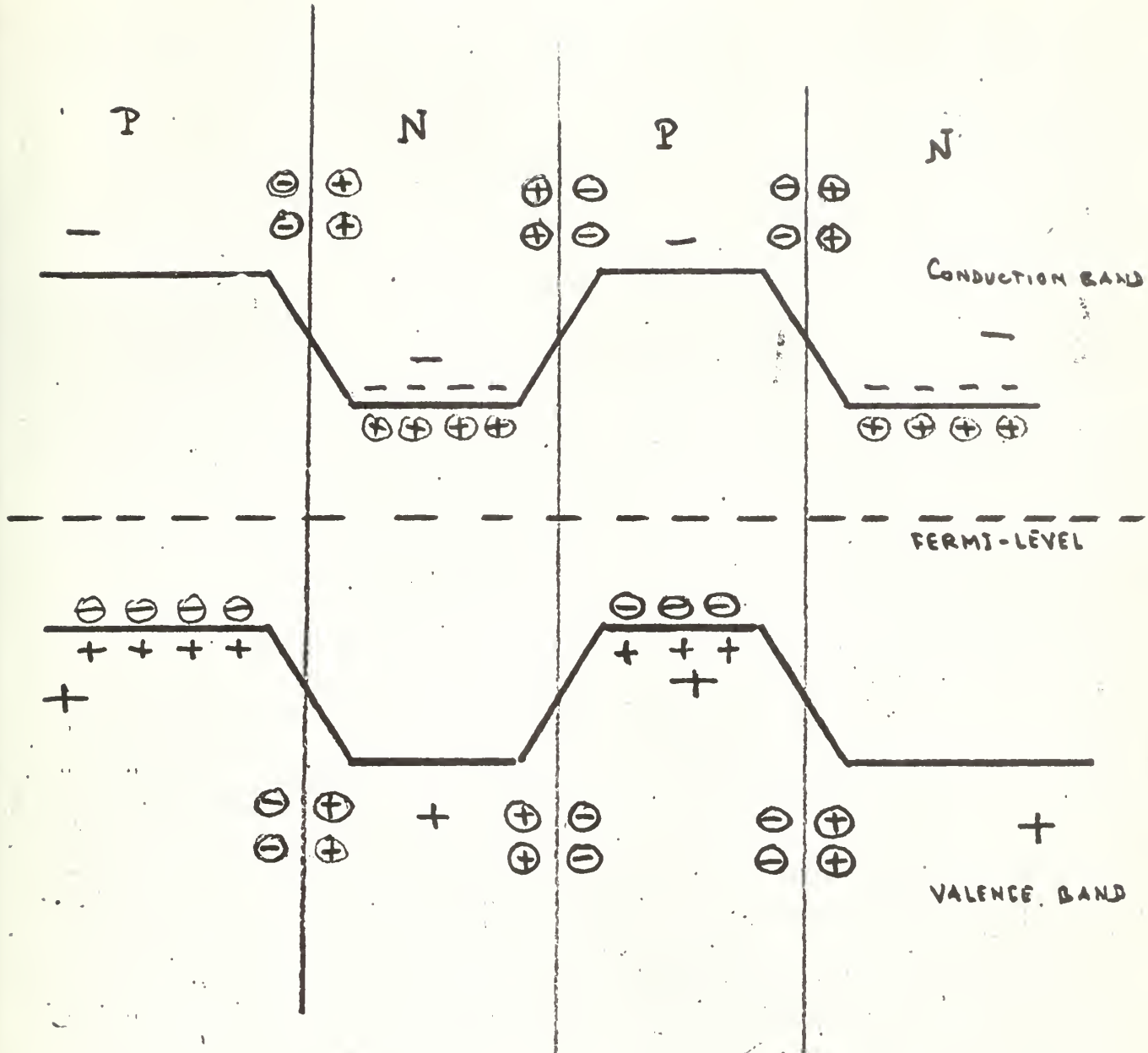
Fig. 1-13 P-N-P-N controlled rectifier,
Region III

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when the sum of the alphas, $\alpha_n + \alpha_p$, is again less than unity which means that the device is switched from region III to region II.

b) By applying a reverse voltage across the SCR. This automatically switches the device to region I as previously discussed.

c) By increasing the holding current. This method is used only in small devices.

The time required for the device to switch from the conducting (Region III) to the blocking region (Region II) is called the "turn off" time.

This is one of the most important parameter in any design circuit, so that we will discuss it in the following paragraphs.

The three regions of operation of the device are shown in Figure I·14. Fig. I-15 shows the effects of increasing gate currents on SCR characteristics.

Fig. 1-14 Typical SCR electrical characteristics

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Fig. 1-15 Effects of increasing gate currents on
SCR Characteristics

I.5 The Turn Off Time of the SCR.

The turn off time of the SCR is defined as the time interval required

for the cell to regain its forward blocking state after forward conduction.

This time is measured from the point where the forward current reaches zero

to the time of reapplication of forward voltage.

When the SCR is in the conduction state, each of the three junctions

are in a condition of forward bias and the two base regions, the center P

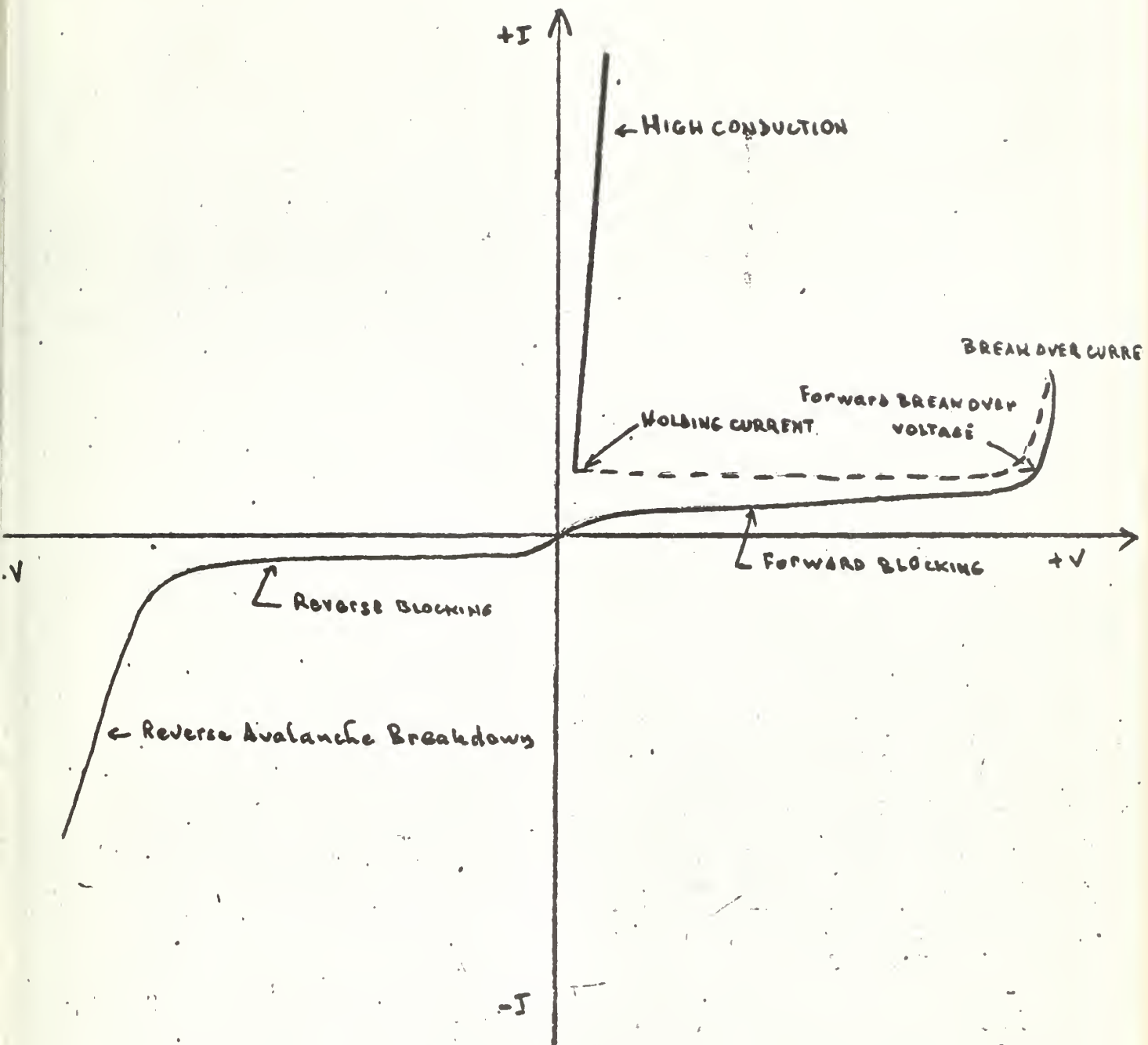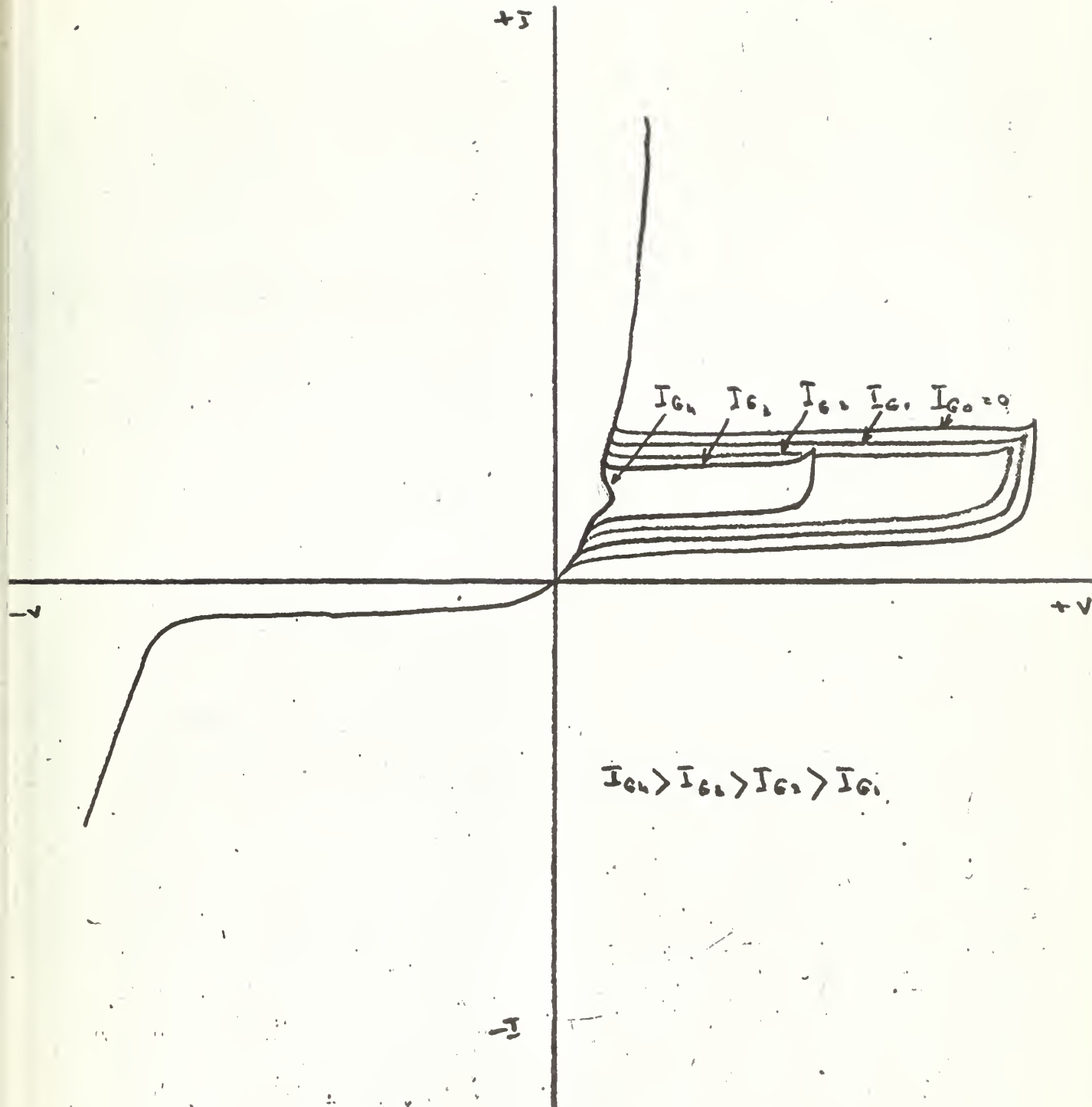and N layers, are heavily saturated with holes and electrons (stored charges).

To turn off the SCR in a minimum time it is necessary to apply a re-

verse voltage. When the reverse voltage is applied, the holes and elec-

trons in the vicinity of the two end junctions (J_1 , J_3) (See Fig. I-16)

will diffuse to these junctions and result in a reverse current in the

external circuit. The voltage across the SCR will remain at about $\pm$ 0.7

volt while an appreciable reverse current builds up.

After the holes and electrons in the vicinity of J_1 and J_3 have been

removed, the reverse current will cease and the junctions J_1 and J_3

will assume a blocking state. The reverse voltage across the SCR will then

increase to a value determined by the external circuit.

Recovery of the SCR is not complete, however, since a high concentra-

tion of holes and electrons would still exist in the vicinity of the center

region (J_2). This concentration decreases by the process of recombina-

tion in a manner which is largely independent of the external bias condi-

tion.

After the hole and electron concentration at J_2 has decreased to a

low value, J_2 will regain its blocking state and a forward voltage (less

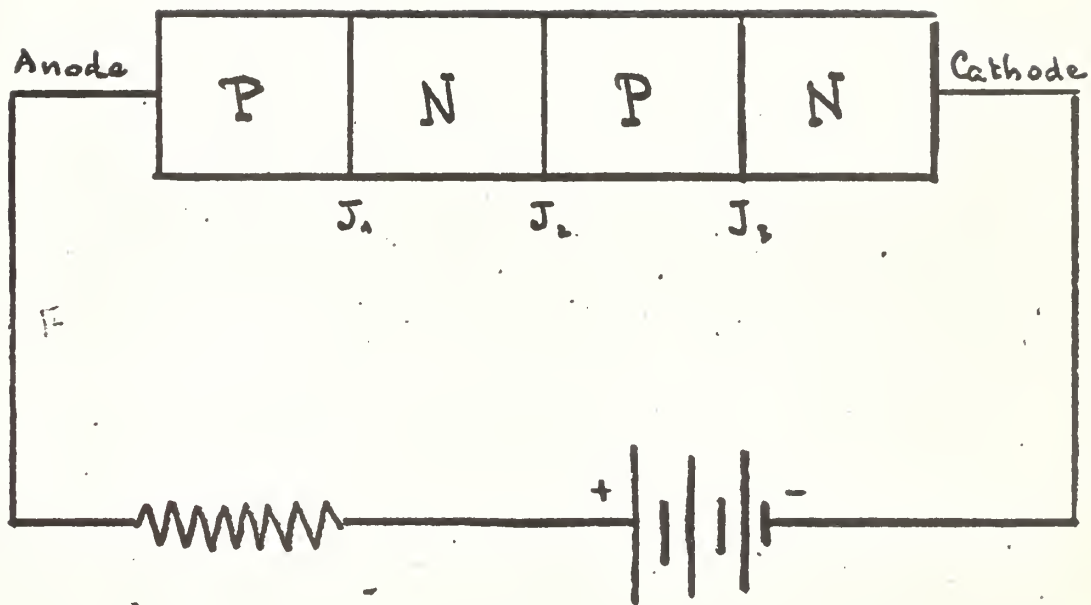than the breakover voltage V_{BO}) may be applied to the SCR without

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Fig. 1-16   P-N-P-N   junction configuration

causing it to turn on. The turn-off time depends on the following factors.

    (1) Junction temperature

    (2) Level of forward current immediately prior to turn-off
       and its rate of decay

    (3) Magnitude of hole storage reverse current permitted to
       flow upon application of inverse voltage and its rate of
       rise.

    (4) Level of inverse voltage immediately prior to reapplication
       of forward blocking voltage.

    (5) Magnitude of reapplied forward blocking voltage following
       turn-off, and its rate of rise.

I.5a Effect of Junction Temperature and Forward Current.

Figure I-17 shows that the variation of turn-off time with junction temperature and forward current.

From Fig. 1-17 we see that at a constant junction temperature, the turn-off time increases with the increasing forward current, the rate of increase is about one microsecond per four amperes. Also at a constant forward current prior to turn-off, the turn-off time increases with the increasing junction temperature, the rate of increase is about one microsecond for 25 degrees C. It is also observed that the rate of decay of the forward current also affects the turn-off time. The faster the rate of decay, the greater is the amount of stored charge and the longer will be the turn-off time.

I.5b Effect of Reverse Current.

The device will not exhibit its normal reverse blocking capability instantaneously because of hole storage within it. The magnitude and duration of the hole storage reverse current depends primarily on the type of

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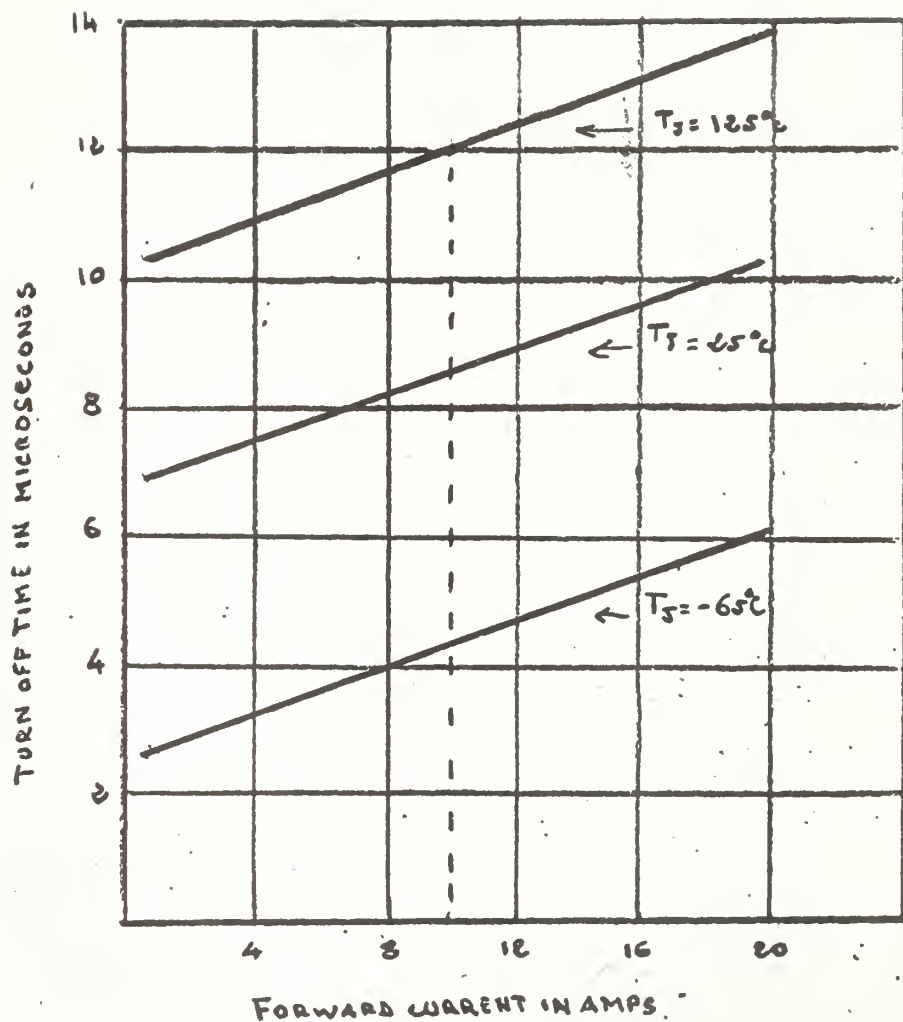
Fig. 1-17 Effect of junction temperature and forward current of turn off time

device and the circuit impedance. If no reverse current is allowed to flow, turn-off time may be as long as 50 to 100 microseconds, but 5 amperes of reverse current will reduce the turn-off time to a value of approximately one tenth of that time. In order to prevent damage to the device, it is also necessary not to exceed the maximum allowable peak reverse current rating specified by the manufacturer. The rate of rise of the reverse current during turn-off is important since it affects the peak of reverse current that will be attained and thus the time duration for reverse recovery. If the rate of rise of reverse current is too slow, then the turn-off time will be increased.

I.5c Effect of Level of Reverse Voltage.

The magnitude of reverse voltage immediately prior to the reapplication of forward blocking voltage is also important. Increased reverse voltage usually decreases turn-off time.

I.5d Effect of the Magnitude of Reapplied Forward Voltage.

When forward blocking voltage is applied to a SCR, the forward blocking capability of the device may be reduced as the rate of application of the voltage is increased. Also the rate of application of reapplied forward blocking voltage affects the turn-off time as shown on Fig. I-18.

Cell type GE C16B

Magnitude of reapplied voltage < 200v

Junction temperature = + 125°c
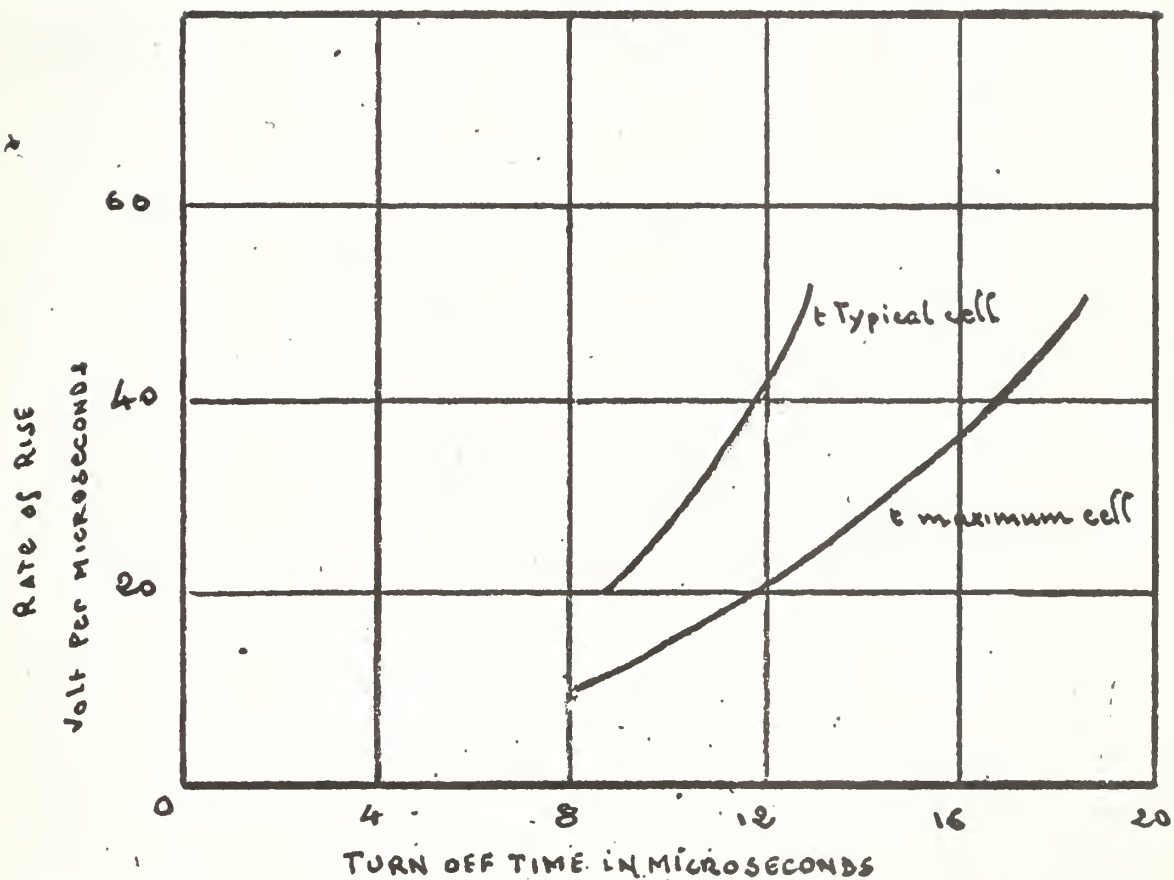
Fig. 1-18 Effect of rate of application of forward
          Blocking

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I.6 Conclusion.

The brief theory of the SCR device has been introduced in this chapter.
In this development, many of the details on solid state physics such as the
band energy theory, the Fermi-level and function theory, the wave particle
duality, the structure of the atoms and so on ......have been omitted.
This does not, however, affect much on the understanding of the SCR opera-
tion. A thorough investigation of the device requires a more tedious study
in solid state physics. The reader who is interested in a more detailed
theory, is referred to the materials listed in the reference chapter at
the end of this paper.

With many advantages over a thyratron, relays, magnetic amplifiers, vacu-
um tubes, power transistor and so on ......, in many industrial, commercial,
and residential applications, the SCR has gained and will gain more of a
reputation for operating reliability, compactness, powerfulness and robust-
ness.

CHAPTER TWO

AN ANALYSIS OF THE PARALLEL INVERTER S.C.R.

II.1 Introduction.

The parallel inverter is the most widely used type of circuit. It requires additional circuit elements to reliably accomplish the commutation process. Its applications have been found in several areas such as aircraft missiles and control instrumentation, where power transistor push-pull inverters have efficiently replaced many of the mechanical methods of converting d.c. battery supplies to higher voltage a.c. supplies.

The SCR used in these inverter circuits acts in a manner similar to the thyratron but it has two great advantages over the thyratron besides its higher current rating, size and weight reduction and robustness, namely:

(1) The turn-off time of the SCR is much smaller than the deionization time of the thyratron. This allows a greater frequency of operation with higher efficiency. (12 μs against up to 3,500 μs).

(2) The voltage drop in the forward direction of the SCR, is also smaller than that of the thyratron ($1 V$ against $10 V$). This gives a more efficient method of inverting low d.c. voltages to very high voltages.

This chapter will concern with the analysis of the parallel inverter in square wave out-put operation for a pure resistance load.

II.2 The Inverter Basic Circuit Operation.

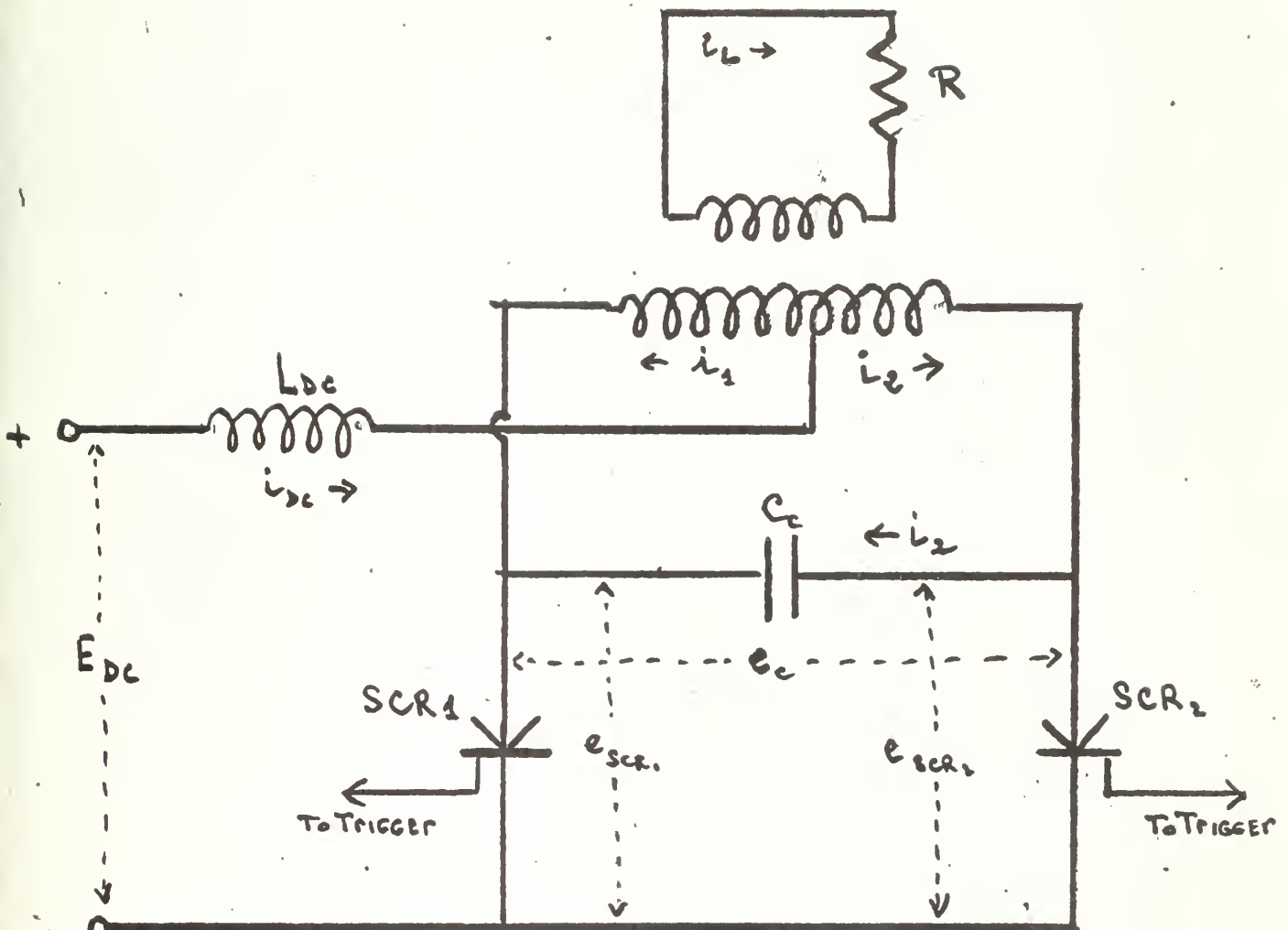The operation of this inverter (See Fig. 2-1) can be briefly explained as follows:

Fig. 2-1 Basic inverter circuit

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When SCR1 is conducting, the capacitor C_c is charged positively on the right hand end. Auto transformer action will produce a voltage of approximately 2E at the anode of SCR2 and across the capacitor. When the next trigger pulse is applied to the gate of SCR2, it will turn on and, as the drop across the conducting SCR (SCR2) is negligible, a voltage of approximately 2E magnitude is applied to the cathode of SCR1, which is the fastest way to turn it off. The capacitor C_c and inductor L_{rc} will maintain a reverse bias across SCR1 long enough for SCR1 to recover to the blocking state. The next trigger pulse will occur at the gate of SCR1 and cause the circuit to revert to the original state. Thus the d.c. current flowing from the supply voltage E alternately to the two halves of the primary of the transformer and produce an a.c. voltage at the load.

II.3 Circuit Analysis.

The following assumptions are made:

(1) The transformer is an ideal one with negligible magnetizing current and negligible winding resistance and reactance.

(2) The inductance has negligible resistance.

(3) SCR1 and SCR2 are ideal controlled rectifiers with zero forward resistance when "on" and infinite resistance when "off".

(4) E_{rc} is a pure d.c. voltage.

(5) The load contains a pure resistance.

(6) The turn ratio between half winding of the primary and secondary is equal to unity.

From Fig. II-1 during the time in which SCR1 is conducting and SCR2 is not conducting, the following equations may be written:

$$i_{DC} = i_1 + i_2 \tag{2-1}$$

$$i_L = i_1 - i_2 \tag{2-2}$$

$$i_2 = i_c = C_c \frac{de_c}{dt} \tag{2-3}$$

$$e_L = \frac{e_c}{2} \tag{2-4}$$

$$e_L = R_L \, i_L \tag{2-5}$$

$$E_{DC} = L_{DC} \frac{di_{DC}}{dt} + e_L = L_{DC} \frac{di_{DC}}{dt} + \frac{e_c}{2} \tag{2-6}$$

$$i_{DC} = \frac{1}{L_{DC}} \int \left(E_{DC} - \frac{e_c}{2} \right) dt = \frac{1}{L_{DC}} \int (E_{DC} - e_L) \, dt \tag{2-7}$$

Subtract (2-2) from (2-1)

$$2 i_2 = i_{DC} - i_L \tag{2-8}$$

(2-4) and (2-3) give

$$i_2 = 2 C_c \frac{de_L}{dt} \tag{2-9}$$

(2-8) and (2-9) give

$$i_{DC} - i_L = 4 C_c \frac{de_c}{dt} \tag{2-10}$$

(2-7) and (2-10) give

$$\frac{1}{L_{DC}} \int (E_{DC} - e_L) \, dt - i_L = 4 C_c \frac{de_c}{dt} \tag{2-11}$$

As previously stated, there is at any time only one SCR conducting, this enables us to draw the following equivalent circuit of the inverter. (See Fig. 2-2).

From Fig. 2-2 we see that the load R_L is now transferred to the primary circuit where $n = \frac{n_2}{n_1}$ (equal to one for the case where $n_2 = n_1$) where n_2 is the number of turns of the secondary winding of the transformer and
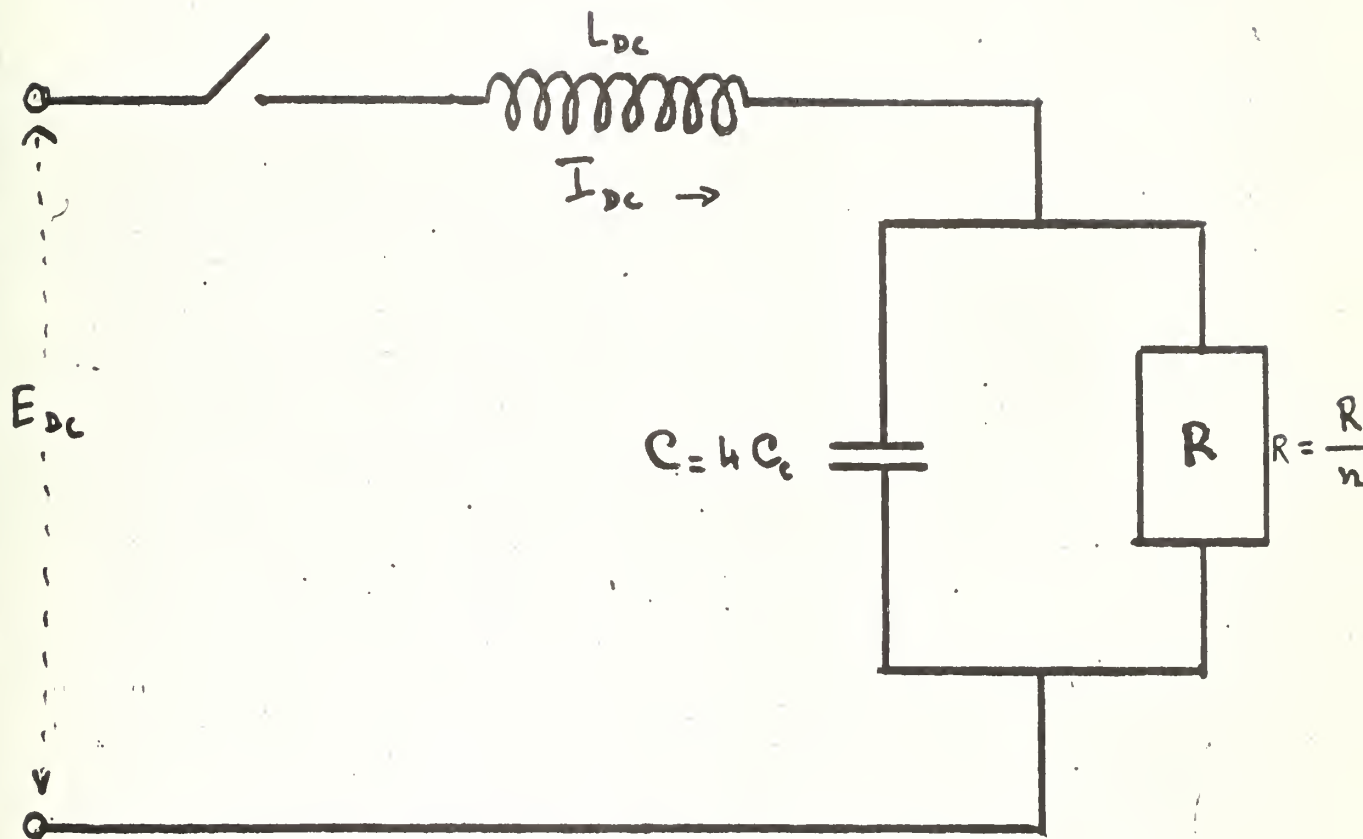
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Fig. 2-2 Equivalent circuit of the inverter

$n_1 =$ half number of turns of the primary winding.

The capacitor which was originally across the whole primary winding now is across only half of the winding, so that its capacitance $= 4 C_c$ (2-12)

The SCR is now represented as a switch. Now take the LaPlace transform of equation (2-5)

$$e_L(s) = R \, i_L(s) \tag{2-13}$$

LaPlace transform of (2-11) gives

$$\frac{E_{DC}}{s^2 L_{DC}} - \frac{e_L(s)}{s \, L_{DC}} + \left[\frac{1}{L_{DC}} \int \left(E_{DC} - \frac{e_c}{2} \right) dt \right]_{at \; t=0^+} - i_L(s) =$$
$$= 4 C_c s \, e_L(s) - 4 C_c e_L(0^+) \tag{2-14}$$

But from (2-7)

$$\frac{1}{L_{DC}} \int \left[\left(E_{DC} - \frac{e_c}{2} \right) dt \right]_{at \; t=0^+} = i_{DC}(0^+) \tag{2-15}$$

Also $e_L(0^+)$ is just equal to $-E_{DC}$ as $e_{L0} = E_{DC}$ of the previous half cycle which has an equal value but opposite sign of that of actual half cycle. Thus

$$e_L(0^+) = -E_{DC} \tag{2-16}$$

Substitute equivalent values just found from (2-15) and (2-16) to (2-14), we obtain:

$$\frac{E_{DC}}{s^2 L_{DC}} - \frac{e_L(s)}{s L_{DC}} + \frac{1}{s} i_{DC}(0^+) - i_L(s) = 4 S C_c \, e_L(s) + 4 C_c \, E_{DC} \tag{2-17}$$

From (2-13)

$$i_L(s) = \frac{e_L(s)}{R} \qquad \left(as \; n = 1 \; so \, that \quad R_L = R_{equivalent} \right) \tag{2-18}$$

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Substitute this value into (2-17)

$$e_L(s)\left(4sc_c + \frac{1}{R} + \frac{1}{sL_{DC}}\right) = \frac{E_{DC}}{s^2 L_{DC}} - 4c_c E_{DC} + \frac{i_{DC}(0^+)}{s} \qquad (2-19)$$

Now from (2-12), $C = 4c_c$ so that (2-19) becomes:

$$e_L(s) \times \left(sc + \frac{1}{R} + \frac{1}{sL_{DC}}\right) = \frac{E_{DC}}{s^2 L_{DC}} - C E_{DC} + \frac{i_{DC}(0^+)}{s} \qquad (2-20)$$

or

$$\frac{e_L(s)\left(s^2 L_{DC} C + s^2 RL_{DC} C + sL_{DC} + R\right)}{sL_{DC} R} = \frac{E_{DC}}{s^2 L_{DC}} + \frac{i_{DC}(0^+)}{s} - C E_{DC} \qquad (2-21)$$

For more convenience, use $L = L_{DC}$ and $E = E_{DC}$, thus

$$e_L(s) = \frac{\frac{ER}{s} + \left[\frac{i_{DC}(0^+)}{s} - CE\right] RSL}{RLCS^2 + LS + R} \qquad (2-22)$$

Divide both numerator and denominator of (2-22) by LRC, we obtain:

$$e_L(s) = \frac{\frac{ER}{LRCS} + \left(\frac{i_{DC}(0^+)}{s} - EC\right)\frac{RSL}{LRC}}{S^2 + \frac{L}{LRC} s + \frac{R}{LRC}} \qquad (2-23)$$

or

$$e_L(s) = \frac{\frac{E}{LCS} + \left(\frac{i_{DC}(0^+)}{s} - CE\right)\frac{S}{C}}{S^2 + \frac{S}{RC} + \frac{1}{LC}} \qquad (2-24)$$

or

$$e_L(s) = \frac{\frac{E}{LC} + (i_{DC}(0^+) - CES)\frac{S}{C}}{S\left(S^2 + \frac{S}{RC} + \frac{1}{LC}\right)} \qquad (2-25)$$

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Now, as previously mentioned $i_{DC}(0^+)$ is the steady state value
of the previous half cycle, i.e., when SCR2 was conducting, thus from the
Fig. 2-2, we have

$$i_{DC}(0^+) = \frac{E}{R} \qquad (2\text{-}26)$$

Substitute this value into (2-25), we obtain:

$$e_L(s) = \frac{\frac{E}{LC}\left(\frac{E}{R} - CES\right)\frac{S}{C}}{S\left(S^2 + \frac{S}{RC} + \frac{1}{LC}\right)} \qquad (2\text{-}27)$$

or

$$e_L(s) = \frac{E}{LCS\left(S^2 + \frac{S}{RC} + \frac{1}{LC}\right)} - \frac{ES}{S^2 + \frac{S}{RC} + \frac{1}{LC}} + \frac{E}{RC\left(S^2 + \frac{S}{RC} + \frac{1}{LC}\right)} \qquad (2\text{-}28)$$

The inverse LaPlace transform of the first part of (2-28) is:

$$e_{L_1}(t) = E\left[1 + \frac{1}{\sqrt{1-\zeta^2}}\, \epsilon^{-\zeta \omega_n t} \sin\left(\omega_n\sqrt{1-\zeta^2}\, t - \psi\right)\right] \qquad (2\text{-}29)$$

where

$$\zeta = \frac{1}{2R}\sqrt{\frac{L}{C}} \qquad (2\text{-}30)$$

$$\omega_n = \frac{1}{\sqrt{LC}} \qquad (2\text{-}31)$$

$$\psi = \tan^{-1}\frac{\sqrt{1-\zeta^2}}{-\zeta} \qquad (2\text{-}32)$$

now let

$$T_c = RC \qquad (2\text{-}33)$$

$$T_L = \frac{L}{R} \qquad (2\text{-}34)$$

and

$$\varphi = \sqrt{\frac{T_c}{T_L} - \frac{1}{4}} \qquad (2\text{-}35)$$

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we have

$$\sqrt{1-\varphi^2} = \sqrt{1 - \frac{1}{4R^2}\frac{L}{C}} = \sqrt{1 - \frac{T_L}{4T_c}} \qquad (2\text{-}36)$$

and
$$w_n\sqrt{1-\varphi^2} = \frac{1}{\sqrt{LC}}\sqrt{\frac{4T_c - T_L}{4T_c}} = \frac{1}{2T_c}\sqrt{\frac{4T_c - T_L}{T_L}} \qquad (2\text{-}37)$$

Thus
$$w_n\sqrt{1-\varphi^2} = \frac{Q}{T_c} \qquad (2\text{-}38)$$

Also
$$\varphi w_n = \frac{1}{\sqrt{T_c T_L}} \times \frac{1}{2R}\sqrt{\frac{L}{C}} = \sqrt{\frac{L}{4R^2 C T_c T_L}} = \frac{1}{2T_c} \qquad (2\text{-}39)$$

Substituting all these values into (2-29), we obtain:

$$e_{L_1}(t) = E\left[1 + \frac{1}{\sqrt{1 - \frac{T_L}{4T_c}}} \, \epsilon^{-\frac{t}{2T_c}} \sin\left(\frac{Qt}{T_c} - \varphi\right)\right] \qquad (2\text{-}40)$$

where
$$\varphi = \tan^{-1}\frac{\sqrt{1-\varphi^2}}{-\varphi} = \tan^{-1}(-2Q) \qquad (2\text{-}41)$$

The inverse LaPlace transform of the 2nd part of (2-28) is:

$$e_{L2}(t) = \frac{w_n^2 \, \epsilon^{-\varphi w_n t}}{\sqrt{1-\varphi^2}} \sin\left(w_n\sqrt{1-\varphi^2}\cdot t + \varphi\right) \qquad (2\text{-}42)$$

where w_n, φ and φ are the same as for the first part, thus:

$$e_{L2}(t) = \frac{E}{\sqrt{1 - \frac{T_L}{4T_c}}} \, \epsilon^{-\frac{t}{2T_c}} \sin\left(\frac{Qt}{T_c} + \varphi\right) \qquad (2\text{-}43)$$

Now for the third and the last part of (2-28), the inverse LaPlace

transform is:

$$e_{L3}(t) = \frac{E/RC}{w_n\sqrt{1-\varsigma^2}} \; \epsilon^{-\varsigma w_n t} \; \sin w_n \sqrt{1-\varsigma^2}\, t \tag{2-44}$$

Where again w_n and ς are the same as for the two first parts, thus:

$$e_{L3}(t) = \frac{E}{T_c \frac{Q}{T_c}} \; \epsilon^{-\frac{t}{2T_c}} \; \sin \frac{Qt}{T_c} \tag{2-45}$$

Thus the total $\quad e_L(t) = e_{L1}(t) + e_{L2}(t) + e_{L3}(t) \quad$ is

$$e_L(t) = E\left[1 + \frac{1}{\sqrt{1+\frac{T_L}{4T_c}}} \; \epsilon^{-\frac{t}{2T_c}} \sin\left(\frac{Qt}{T_c} - \psi\right)\right]$$

$$- E\; \epsilon^{-t/2T_c} \sin\left(\frac{Qt}{T_c} + \psi\right) + \frac{E}{Q}\; \epsilon^{-\frac{t}{2T_c}} \sin\frac{Qt}{T_c} \tag{2-46}$$

or $\quad e_L(t) = \frac{E}{\sqrt{1-\frac{T_L}{4T_c}}} \; \epsilon^{-t/2T_c}\left[\sin\left(\frac{Qt}{T_c} - \psi\right) - \sin\left(\frac{Qt}{T_c} + \psi\right)\right]$

$$+ E \quad + \frac{E}{Q}\; \epsilon^{-t/2T_c} \sin\frac{Qt}{T_c} \tag{2-47}$$

but $\quad \sin\left(\frac{Qt}{T_c} - \psi\right) - \sin\left(\frac{Qt}{T_c} + \psi\right) = -2\cos\frac{Qt}{T_c}\sin\psi \tag{2-48}$

from $(2-41)$

$$\frac{\sin\psi}{\cos\psi} = -2Q = \frac{\sin\psi}{\sqrt{1-\sin^2\psi}} \quad \rightarrow \quad \sin\psi = -2Q\sqrt{1-\sin^2\psi} \quad \rightarrow \quad \sin^2\psi = 4Q^2\left(1-\sin^2\psi\right)$$

$$\therefore \quad \sin\psi = \frac{2Q}{\sqrt{1+4Q^2}} \tag{2-49}$$

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but $\quad Q = \sqrt{\dfrac{T_c}{T_L} - \dfrac{1}{4}}$ $\qquad$ from (2-35), thus (2-49) becomes:

$$\sin \psi = \frac{2Q}{2\sqrt{\dfrac{T_c}{T_L}}} \tag{2-50}$$

Substitute this value of $\sin \psi$ into (2-48), we obtain;

$$\sin\left(\frac{Qt}{T_c} - \psi\right) - \sin\left(\frac{Qt}{T_c} + \psi\right) = -2\cos\frac{Qt}{T_c} \times \frac{Q}{\sqrt{\dfrac{T_c}{T_L}}} = \frac{-4Q}{\sqrt{\dfrac{4T_c}{T_L}}} \cos \frac{Qt}{T_c} \tag{2-51}$$

Substitute this value into (2-46), we obtain:

$$e_L(t) = E\, \epsilon^{-t/2T_c}\left[\frac{1}{\sqrt{\dfrac{4T_c - T_L}{4T_c}}}\left(\frac{-4Q}{\sqrt{\dfrac{4T_c}{T_L}}}\cos\frac{Qt}{T_c}\right)\right] + E + \frac{E}{Q}\epsilon^{-t/2T_c}\sin\frac{Qt}{T_c}$$

or $\quad e_L(t) = E\left[1 + \epsilon^{-t/2T_c}\left(-2\cos\frac{Qt}{T_c} + \frac{1}{Q}\sin\frac{Qt}{T_c}\right)\right] \tag{2-52}$

Equation (2-52) represents the variation of the load voltage which, from Fig. II-2, is at the same time the variation of the commutating voltage during the half cycle.

The graph of Equation (2-52) is shown on Fig. II-3.

From figure II-3, we see that the load voltage has a steady state value equal to E and an initial value of - E, it also has a transient effect due to the sine and cosine terms with an exponential envelope due to the $\epsilon^{-t/2T_c}$ term.

Next we have to calculate the current flowing through the conducting SCR during the half cycle, namely $\dot{i}_{pc}$. We have from equation (2-7) in taking its LaPlace transform:

$$\dot{i}_{pc}(s) = \frac{1}{L}\left(\frac{E}{s^2} - \frac{e_{L}(s)}{s}\right) + \frac{\dot{i}_{pc}(o^+)}{s} \tag{2-53}$$
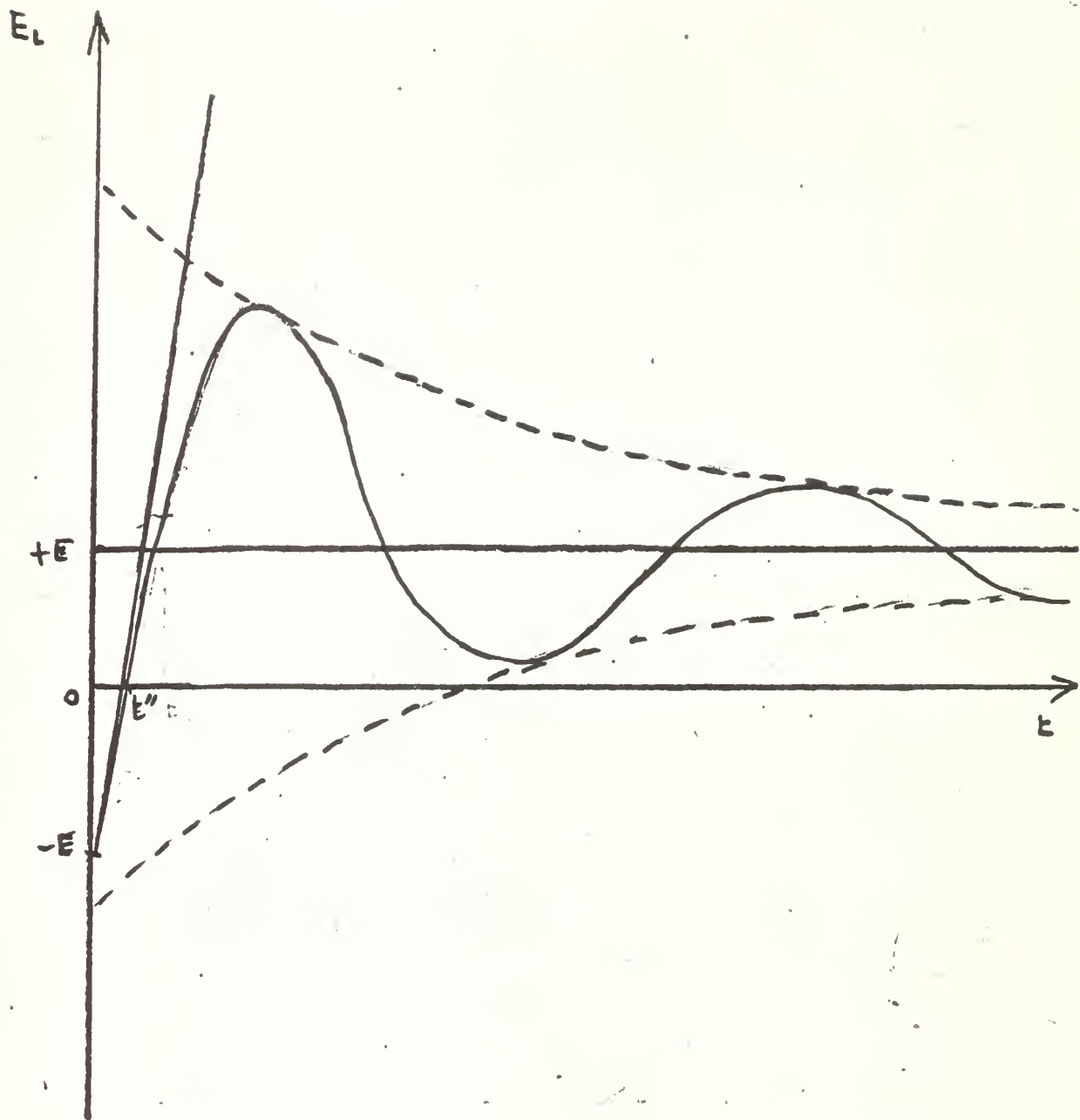
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Fig. 2-3 Variation of the commutating voltage during the
          half cycle

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Where $e_L(s)$ is given by (2-28) and $i_{DC}(0^+) = \frac{E}{R}$ as previously found.

Using these above values of $e_L(s)$ and $i_{DC}(0^+)$ we can write (2-53) as follows:

$$i_{DC}(s) = \frac{1}{L}\left[\left(\frac{E}{s^2} - \frac{E/LC}{s^2(s^2 + \frac{s}{RC} + \frac{1}{LC})}\right) + \frac{SE}{s(s^2 + \frac{s}{RC} + \frac{1}{LC})} - \frac{E/RC}{s(s^2 + \frac{s}{RC} + \frac{1}{LC})}\right.$$
$$\left. + \frac{E}{RS}\right] \quad (2-54)$$

The inverse LaPlace transform of (2-54) has five components as follows:

$$i_{DC_1}(t) = \frac{E}{L}t \quad (2-56)$$

$$i_{DC_2}(t) = \frac{-E}{L}\left[t - \frac{2\varphi}{\omega_n} + \frac{1}{\omega_n\sqrt{1-\varphi^2}} \epsilon^{-\varphi\omega_n t} \sin\left(\omega_n\sqrt{1-\varphi^2}\, t - \psi_2\right)\right] \quad (2-57)$$

where, as before $\varphi = \frac{1}{2R}\sqrt{\frac{L}{C}}$, $\omega_n = \frac{1}{\sqrt{LC}}$

and $\psi_2 = 2\tan^{-1}\frac{\sqrt{1-\varphi^2}}{-\varphi}$ $\quad (2-58)$

or $\psi_2 = 2\tan^{-1}(-2Q)$ (See Equation 2-41)

$$i_{DC_3}(t) = \frac{E/L}{\omega_n\sqrt{1-\varphi^2}} \epsilon^{-\varphi\omega_n t} \sin\omega_n\sqrt{1-\varphi^2}\, t \quad (2-59)$$

$$i_{DC_4}(t) = -\frac{E}{R}\left[1 + \frac{1}{\sqrt{1-\varphi^2}} \epsilon^{-\varphi\omega_n t} \sin\left(\omega_n\sqrt{1-\varphi^2}\, t - \psi_4\right)\right] \quad (2-60)$$

Where $\psi_4 = \tan^{-1}\frac{\sqrt{1-\varphi^2}}{-\varphi} = \tan^{-1}(-2Q)$ $\quad (2-61)$

and finally: $\quad i_{DC5}(t) = \dfrac{E}{R}$

The total $\quad i_{DC}(t) \quad$ is thus: $\quad i_{DC}(t) = i_{DC_1}(t) + i_{DC_2}(t) + i_{DC_3}(t) + i_{DC_4}(t) + i_{DC_5}(t)$

or $\quad i_{DC}(t) = \dfrac{E}{L}t - \dfrac{E}{L}\left[t - \dfrac{2}{2R}\sqrt{\dfrac{L}{C}} \times \sqrt{LC} + \dfrac{1/Q}{T_c} e^{-t/2T_c} \sin\left(\dfrac{Qt}{T_c} - \Psi_2\right) \right]$

$\qquad -\dfrac{E}{R}\left[1 + \dfrac{1}{\sqrt{1 - \dfrac{T_L}{4T_c}}} \; e^{-t/2T_c} \sin\left(\dfrac{Qt}{T_c} - \Psi_4\right) \right] + \dfrac{E}{R}$ $\qquad$ (2-62)

or $\quad i_{DC}(t) = \dfrac{E}{R} - \dfrac{E}{L\dfrac{Q}{T_c}} e^{-t/2T_c} \sin\left(\dfrac{Qt}{T_c} - \Psi_2\right) + \dfrac{E}{L\dfrac{Q}{T_c}} e^{-t/2T_c} \sin\dfrac{Qt}{T_c}$

$\qquad -\dfrac{E}{R} - \dfrac{E}{R\sqrt{1 - \dfrac{T_L}{4T_c}}} \; e^{-t/2T_c} \sin\left(\dfrac{Qt}{T_c} - \Psi_4\right) + \dfrac{E}{R}$ $\qquad$ (2-63)

let $\dfrac{t}{2T_c} = a \quad , \quad \dfrac{Qt}{T_c} = b \quad , \quad$ (2-63) becomes:

$i_{DC}(t) = \dfrac{E}{L\dfrac{Q}{T_c}} e^{-a}\left[\sin b - \sin(b - \Psi_2) \right] - \dfrac{E}{R\sqrt{1 - \dfrac{T_L}{4T_c}}} e^{-a} \sin(b - \Psi_4) + \dfrac{E}{R}$ $\qquad$ (2-64)

From the identity $\quad \sin x - \sin y = 2 \sin\left(\dfrac{x-y}{2}\right) \cos\left(\dfrac{x+y}{2}\right)$

we have $\sin b - \sin(b - \Psi_2) = 2 \sin\dfrac{\Psi_2}{2}\left(\cos b \cos\dfrac{\Psi_2}{2} + \sin b \sin\dfrac{\Psi_2}{2} \right)$ $\qquad$ (2-65)

Now $\quad \Psi_2 = 2 \tan^{-1}(-2Q) \quad \rightarrow \quad \dfrac{\Psi}{2} = \tan^{-1}(-2Q)$ $\qquad$ (2-66)

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$$\therefore \quad \frac{\sin \psi/2}{\cos \psi/2} = -2Q \quad \rightarrow \quad \cos \psi/2 = \sqrt{\frac{T_L}{4T_c}} \tag{2-67}$$

also $\quad \dfrac{\sin \psi/2}{\sqrt{1-\sin^2 \psi/2}} = -2Q \rightarrow \sin \psi/2 = \dfrac{2Q}{\sqrt{1+4Q^2}}$ \hfill (2-68)

Substitute the above values of $\sin \psi/2$ and $\cos \psi/2$ into (2-65), we obtain:

$$\sin b - \sin(b-\psi_2) = 2\left[\frac{2Q}{\sqrt{1+4Q^2}}\left(\frac{1}{\sqrt{1+4Q^2}}\cos b + \frac{2Q}{\sqrt{1+4Q}}\sin b\right)\right]$$

$$\therefore \quad \sin b - \sin(b-\psi_2) = \frac{4Q}{1+4Q^2}\left(\cos b + 2Q\sin b\right) \tag{2-69}$$

Similarly $\quad \sin(b-\psi_4) = \sin b \cos \psi_4 - \cos b \sin \psi_4$ \hfill (2-70)

where $\quad \psi_4 = \tan^{-1}(-2Q)$ $\quad$, thus $\sin \psi_4 = \dfrac{2Q}{\sqrt{1+4Q^2}}$ \hfill (2-71)

and $\quad \cos \psi_4 = \cos\left(\frac{\psi_2}{2}\right) = \dfrac{1}{\sqrt{1+4Q^2}}$ \hfill (2-72)

Using these expressions in equation (2-70), we obtain:

$$\sin(b-\psi_4) = \sin b \times \frac{1}{\sqrt{1+4Q^2}} - \cos b \times \frac{2Q}{\sqrt{1+4Q^2}}$$

$$= \frac{1}{\sqrt{1+4Q^2}}\left(\sin b - 2Q\cos b\right) \tag{2-73}$$

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Now substitute all the new values just found into (2-64), we obtain:

$$i_{DC}(t) = \frac{E}{L\frac{Q}{T_c}} \, \epsilon^{-a} \left[\frac{4Q}{1+4Q^2} (\cos b + 2Q \sin b) \right]$$
$$- \frac{E}{R\sqrt{1-\frac{T_L}{4T_c}}} \, \epsilon^{-a} \frac{1}{\sqrt{1+4Q^2}} \left(\sin b - 2Q \cos b \right) + \frac{E}{R} \qquad (2\text{-}74)$$

As $1+4Q^2 = 4\frac{T_c}{T_L}$ thus (2-74) can be simplified as follows:

$$i_{DC}(t) = \epsilon^{-a} \frac{E}{R} (\cos b + 2Q \sin b) - \frac{E}{2RQ} \left(\sin b - 2Q \cos b \right) + \frac{E}{R} \qquad (2\text{-}75)$$

or $$i_{DC}(t) = \frac{E}{R} \left[1 + \epsilon^{-a} \sin b \left(2Q + \frac{1}{2Q} \right) \right] \qquad (2\text{-}76)$$

Now plug back the real values of a and b into (2-76), we have:

$$i_{DC}(t) = \frac{E}{R} \left[1 + \epsilon^{-t/2T_c} \times \frac{2(Q^2 + \frac{1}{4})}{Q} \sin \frac{Qt}{T_c} \right] \qquad (2\text{-}77)$$

The graph of Equation (2-77) is shown in Figure 2-4 .

From the curve of Figure (2-4), we can see that for all value of $\frac{T_c}{T_L} > \frac{1}{4}$ which gives Q a real value, the current flowing through the SCR during the conduction has the form of a damped sine wave oscillation about the reference level $i(t=0) = \frac{E}{R}$.

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In order for the inverter to work properly, the SCR must fulfill two main conditions, first it must be maintained in the conducting period during the whole half-cycle and second, it must be turned off at the end of the conducting half cycle.

II.4 Condition for Maintaining Conduction.

From Figure 2-4, we can see that SCR can be turned off during the switching transient period, i.e., when the $i_{DC}(t)$ curve touches the zero current axis. This can only happen when the first minimum of the oscillation is so great that it touches the zero current axis.

Supposing this to occur, let us call t' the time at which $i_{DC}(t) = 0$ this time t' is related by equation (2-77) and Figure 2-4 as follows:

$$\frac{Q}{T_c} t' = \frac{3\pi}{2} \qquad (2\text{-}78)$$

or

$$\frac{t'}{2T_c} = \frac{3\pi}{4Q} \qquad (2\text{-}79)$$

Substituting this value into Equation (2-77), we obtain:

$$i_{DC}(t) = \frac{E}{R}\left[1 - \frac{2(Q^2 + \frac{1}{4})}{Q} \, \epsilon^{-\frac{3\pi}{4Q}}\right] \qquad (2\text{-}80)$$

Thus $i_{DC}(t) = 0$ when $\dfrac{2(Q^2 + \frac{1}{4})}{Q} \, \epsilon^{3\pi/4Q} = 1$

or

$$\frac{3\pi}{4Q} = L_n \frac{2(Q^2 + \frac{1}{4})}{Q} \qquad (2\text{-}81)$$

Equation (2-81) can be solved graphically by given Q different values then solve for $\dfrac{3\pi}{4Q}$ and for $L_n \dfrac{2(Q^2 + \frac{1}{4})}{Q}$
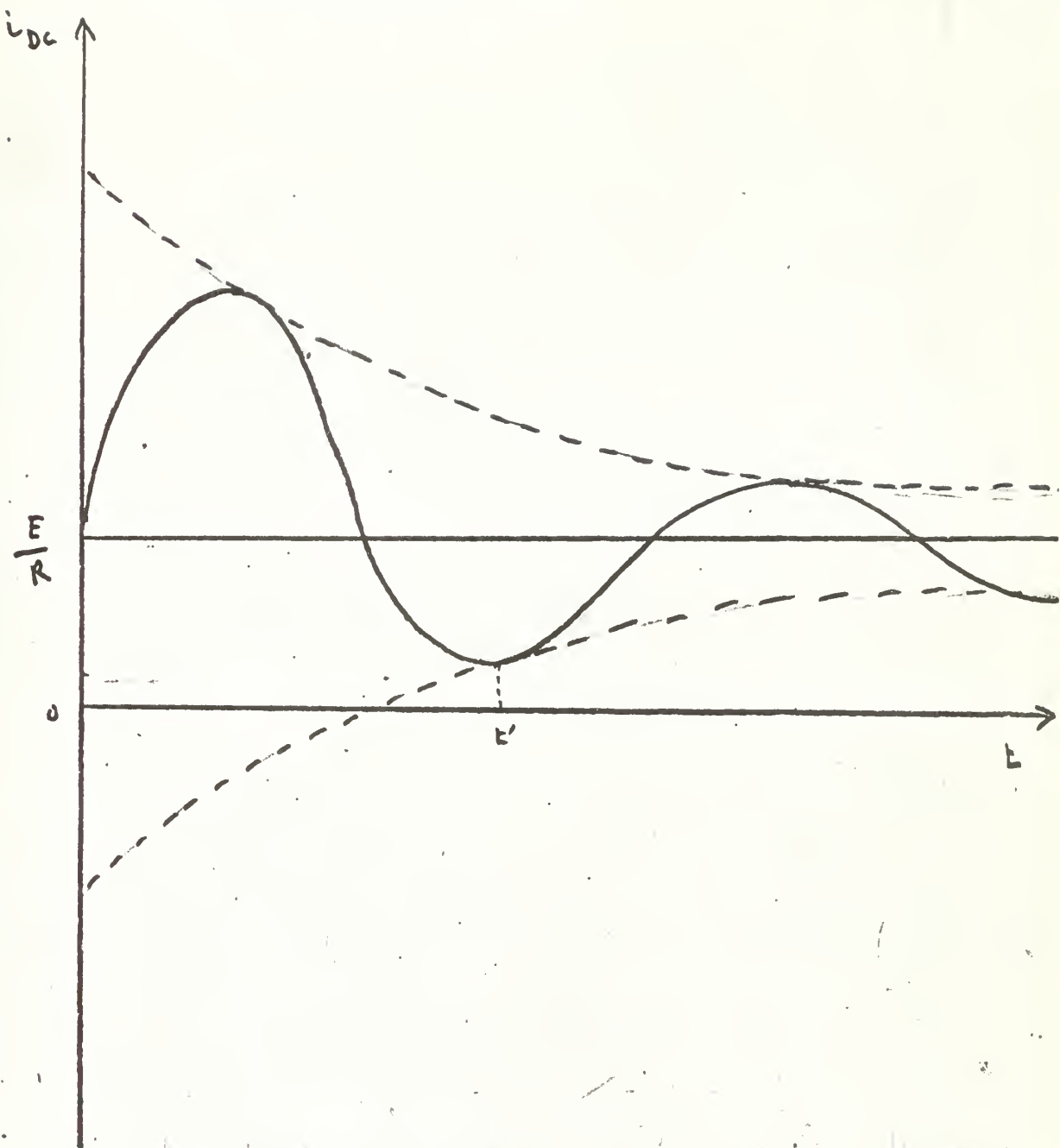
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Fig. 2-4   Variation of the current flowing through the
           SCR during conduction

Figure 2-5 is the graphical solution of (2-81) using $Q^2 + \frac{1}{4} = \frac{T_c}{T_L}$ as parameter.

From the graphical solution given we can see that the current flowing through the SCR during conduction cannot be cut off when $\frac{T_c}{T_L} < 3.28$

But when using equation (2-78), we neglected the slight effect of the exponential decay on the position of the first minimum of the current curve. Thus a value of $\frac{T_c}{T_L} < 3.24$ given by reference 11 seems to be more accurate.

Now the condition to maintain the conduction during the half cycle can be written as:

$$0.25 < \frac{T_c}{T_L} < 3.24 \qquad (2\text{-}82)$$

II.5 Condition for Turn-Off.

Failure of turn off means short circuiting and damaging the inverter, so the SCR must be maintained in the reverse biased portion long enough for it to completely turn off.

From Figure 2-3, we can see that the time during which the commutating voltage is negative is represented by t'', now if we ignore the very slight curvature of the first part of the voltage curve, we can solve t'' by taking the gradient of this curve at $t = 0$, thus from (2-52)

$$\frac{de}{dt}\Big|_{t=0} = \frac{2E}{T_c} \qquad (2\text{-}83)$$

and from Figure 2-3,

$$\frac{de}{dt}\Big|_{t=0} = \frac{E}{t''} \qquad (2\text{-}84)$$

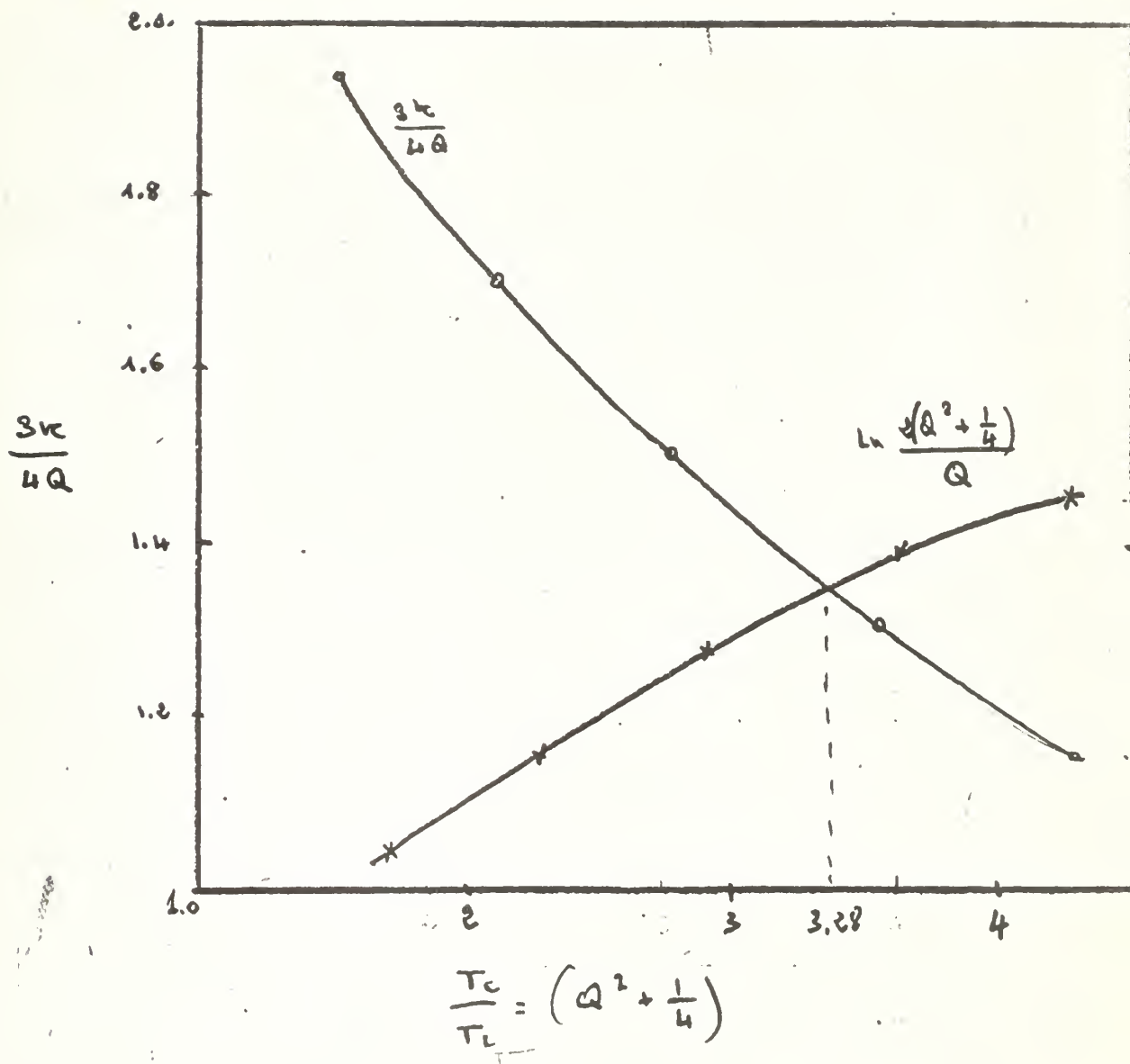Equate (2-83) and (2-84), we obtain: $t'' = \frac{T_c}{2}$

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Fig. 2-5 Graphical solution for the limiting of
$$\frac{T_c}{T_L}$$

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Thus the SCR will turn off successfully if $\frac{T_c}{2} > t_{off}$ (2-85)

where t_{off} is the turn off time of the specified SCR given by its data sheet.

It is worth noting that by ignoring the curvature of the first part of the curve in Figure 2-3, we have given more margin to the completion of the turn off time which is a good approximation.

II.6 Square Wave Operation.

If the switching transient has died out before the triggering occurs, then the boundary conditions at the beginning and end of the half cycle are matched. In this case the output voltage has a square wave form which is the most efficient process as the loss during commutation is the smallest.

As previously mentioned, inverter devices with high frequency of operation are highly desirable because of a reduction in size and weight of the transformer. The frequency is limited, however, by the condition for the SCR to turn off successfully, i.e., by the condition satisfying equation (2-85).

The retriggering can be effectively applied when the exponential has decayed to less than 5% of its reference value, i.e., within 5% of the reference voltage of E or the current level of $\frac{E}{R}$.

Thus from equations (2-52) and (2-77), (the exponential part given by $\epsilon^{-t/2T_c}$), the above condition can be expressed as: $\epsilon^{-t/2T_c} = 0.05 = \epsilon^{-3}$

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which is the same as saying

$$T > 6 T_c \qquad (2\text{-}86)$$

where T : half cycle period and $T_c = RC$,

or the maximum repetition rate f_{max} is given by:

$$f_{max} = \frac{1}{2 T_{min}} = \frac{1}{12 RC} \qquad (2\text{-}87)$$

II.7   Summary of the Analytical Results.

Rewrite equation (2-82)

$$0.25 < \frac{T_c}{T_L} < 3.24$$

This gives the desired mode of operation.

When $\frac{T_c}{T_L} < 0.25$ the switching transient is heavily damped
and the output wave form has an exponential leading front which is un-
desirable.   This also decreases the efficiency as we have more commutating
loss due to the heavy damping.   At the same time the inverter lacks the
ability to adjust itself to abrupt changes of load because of the large
transient effect.

When $\frac{T_c}{T_L} > 3.24$ the current flows in pulses from the supply,
and hence the mode is inefficient and generally undesirable.

The square wave operation is the most efficient and desirable mode.
For the SCR usually used in inverter the turn off time is about 12 μs ,
from equation (2-85) $\frac{T_c}{2} > t_{off}$ and equation (2-86), $T > 6 T_c$.

   or $\qquad T > 12 \, t_{off}$

thus the maximum frequency that can be used is:

$$\frac{1}{2T} = \frac{1}{24 t_{off}} \quad \text{or} \quad f_{max} = \frac{1}{24 t_{off}} = \frac{10^6}{288}$$

$$\therefore \quad f_{max} \cong 3.5 \, kcs$$

It should be noted that the higher the operation frequency, the lighter is the weight of the transformer and the higher will be the commutation loss, so that a frequency between 500 and 2000 cycles per second is the most practical operating frequency for the square wave mode.

II.8 Trigger Requirements.

Triggering circuits of various types can be used to give a steep wave front applied alternately to the SCR gates. The duration of the gate signal is such that it must be maintained until the load current through the SCR exceeds the hold-in value for the SCR. If the trigger signal is lost, one of the SCR remains on and the current is limited only by the circuit and supply resistance.

Transistor multivibrators, saturable reactors, unijunction and other transistor trigger generator circuit can be used as trigger circuit to drive SCR inverters.

II.9 Transformer Requirements.

The choice of the transformer is quite critical because of the saturation of the transformer during starting. If the initial flux in the transformer is near its peak value and the circuit is started with the flux increasing further, the transformer may saturate and prevent commutation of the circuit at the next trigger pulse. This situation can be prevented by using a larger transformer or by shortening the duration time of the first half cycle of operation.

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A transformer having a toroidal, square loop magnetic core often causes random starting difficulties because of the residual effect in the core. On the other hand the transformer with an air gap and operating at lower flux density will give less starting difficulties.

It is considered to be safe to operate at only about one third of the saturation flux density of the transformer core.

II.10 Conclusion.

This chapter has presented an analysis of the parallel inverter operation with pure resistance load. The analysis shows that there are three modes of operation, two of which are undesirable, because of reasons previously mentioned.

This analysis has used a similar approach to the one mentioned in the bibliography.

By using the LaPlace transform, we simplified much of the analysis .

The introduction of the SCR in the inverter circuit allowed us to simplify the analysis in comparison with that of the thyratron given by reference 11 of the bibliography.

In the thyratron circuit since the deionization time may be as much as $3500\,\mu s$ in comparison with the turn off time of the SCR of about $10\,\mu s$, the method used here becomes inadmissible, because far from being able to ignore the curvature of the first part of the voltage wave form of Fig. 2-3, the circuit needs to be built so that a sharp curvature can be produced in order to turn off the thyratron successfully. Therefore a heavily damped switching transient is necessary which leads to both inductance and capacitance parameters.

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The analysis can be carried out by the extremely tedious method of plotting the current and voltage wave forms according to various frequency dependent inductance and capacitance parameters and then plotting the required commutating ratio (corresponding to $\frac{t'}{T}$ in our case) against the capacitance parameters while holding the inductance parameters fixed. This would require too much time and work and is therefore of little value in practical circuit design.

An experimental set up will be given in the next chapter.

EXPERIMENTAL SET UP OF A PARALLEL INVERTER

III.1 Experimental set up.

The circuit diagram of a parallel inverter is shown in Figure 3-1 where we can see two parts: the trigger and the inverter circuit itself.

III.1a Trigger circuit.

The trigger circuit is a two transistor free running, multivibrator. This multivibrator can give a square wave from a low impedance source, which on differentiation by the coupling capacitor SCR input impedance network produces positive pulses of about 2 volts, 180° out of phase on the gates of the SCR. The magnitude of the pulses depends on the value of the supply voltage, the frequency can be varied between about 100 cps to about 5,000 cps by changing the capacitors C1 and C2. (See Figure 3-2).

III.1b The inverter circuit.

The inverter circuit is shown in Figure 3-3 with all data of the components. The electrolytic capacitor across the supply enables it to accept power as well as supply power. The series resistance following the electrolytic capacitor is used as a voltage divider. The transformer data is also given at the bottom of Figure 3-3.

The choice of the ballast inductance, commutation capacitor and load resistance is made in such a way as to satisfy the three modes of operation given in Chapter II, namely, when $0.25 < \dfrac{T_c}{T_L} < 3.24$

Three different frequencies are used:

>   1 - The highest one to give the beginning of the deformation of
>   the square wave output.

2 - The normal frequency to give a fairly good square wave out-

put.

3 - The lowest frequency to give a square wave output, below that

frequency the device fails to operate because of transformer

saturation.

III.2 Experimental results.

Experimental results are showing by the enlarged photographs at the

end of this chapter. The values of the different components when changed are

noted at the bottom of each figure.

III.3 Discussion of the results.

The experimental results checked fairly close with that of the anal-

ysis given in chapter two. It is observed however, that the lower limit of

equation $0.25 < \dfrac{T_c}{T_L} < 3.24$ have been used with no load condition. The device

fails to work at value $0 < \dfrac{T_c}{T_L} < .25$. The failure is believed to come

from the saturation of the transformer core. The higher limit was obtained

with $\dfrac{T_c}{T_L} = 3.4$, the result did show a large oscillation which is not, how-

ever, big enough to cause pulse delivery from the supply. In order to reach

the pulse delivery, we need to increase excessively the value of the re-

sistance and keep the commutation capacitor fixed. This results in a value

of $\dfrac{T_c}{T_L}$ much larger than 3.24.

The waveforms of the voltage across the SCR are observed to have more

oscillations than that of the output voltage, which is reasonable because

of the transformer reflection.

III.4 Conclusions.

The experimental results are satisfactory. It is observed that the

choice of the commutation capacitor is more critical than that of the bal-

last inductance and load resistance. With a capacitor of $2\,\mu$F or above,

operations are satisfactory for a large range of load resistance, including
no load, and of ballast inductance (from about 30 μH up to about 500 μH).
The CII SCR are well suited for inverter application up to a kilowatt power
output. The maximum frequency for square wave output is about 5,000 cps,
and that for sinewave output is about 10,000 cps.

3-1
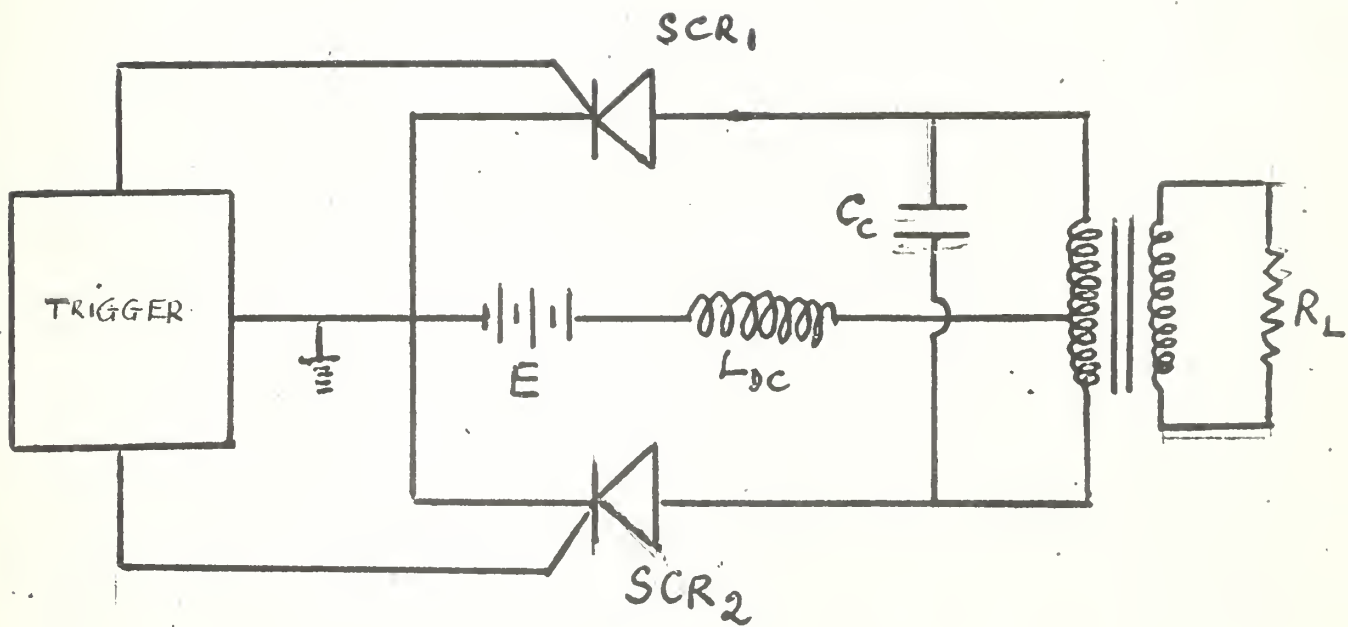
Fig. 3-1 Basic parallel inverter circuit
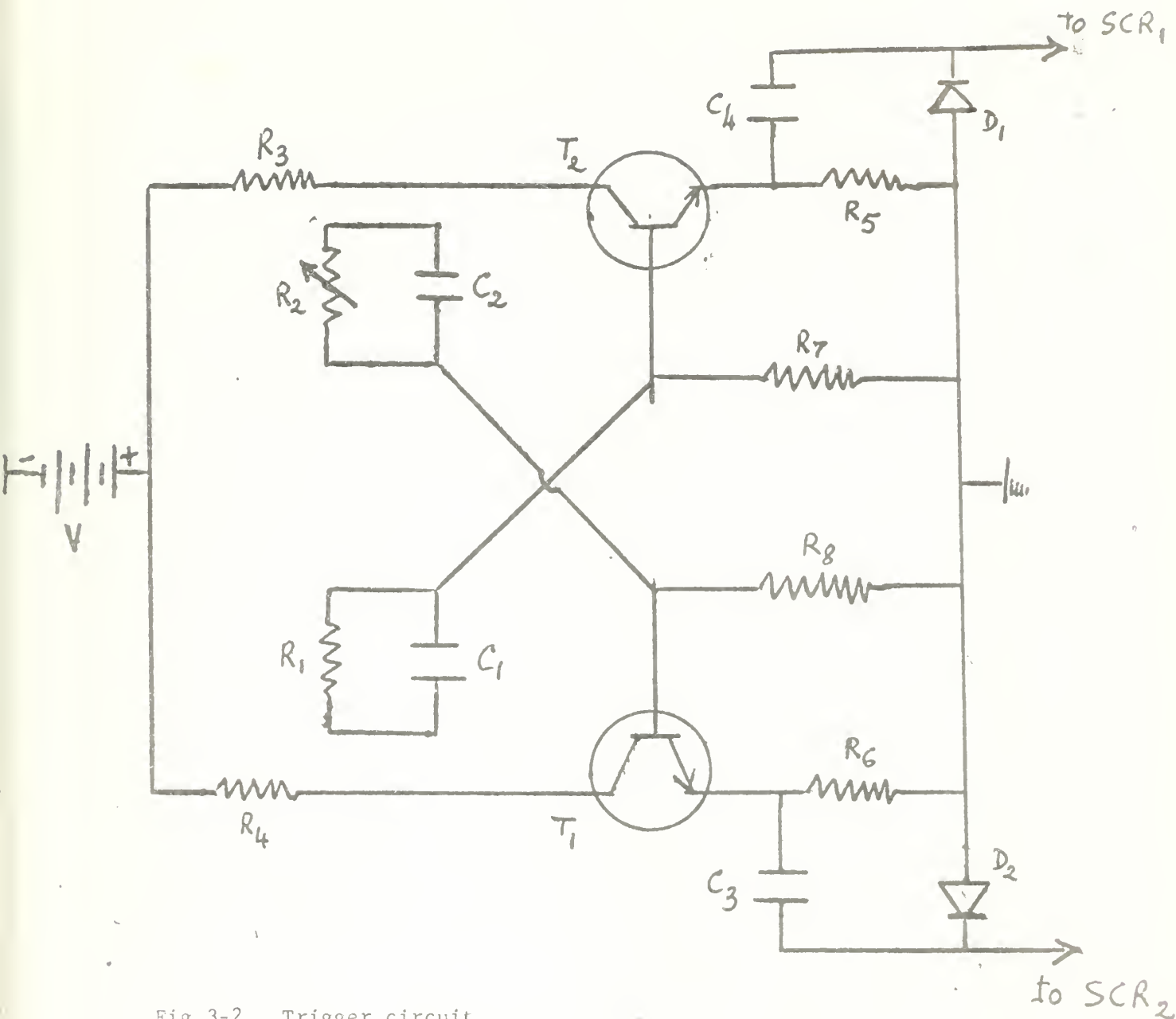
3-1
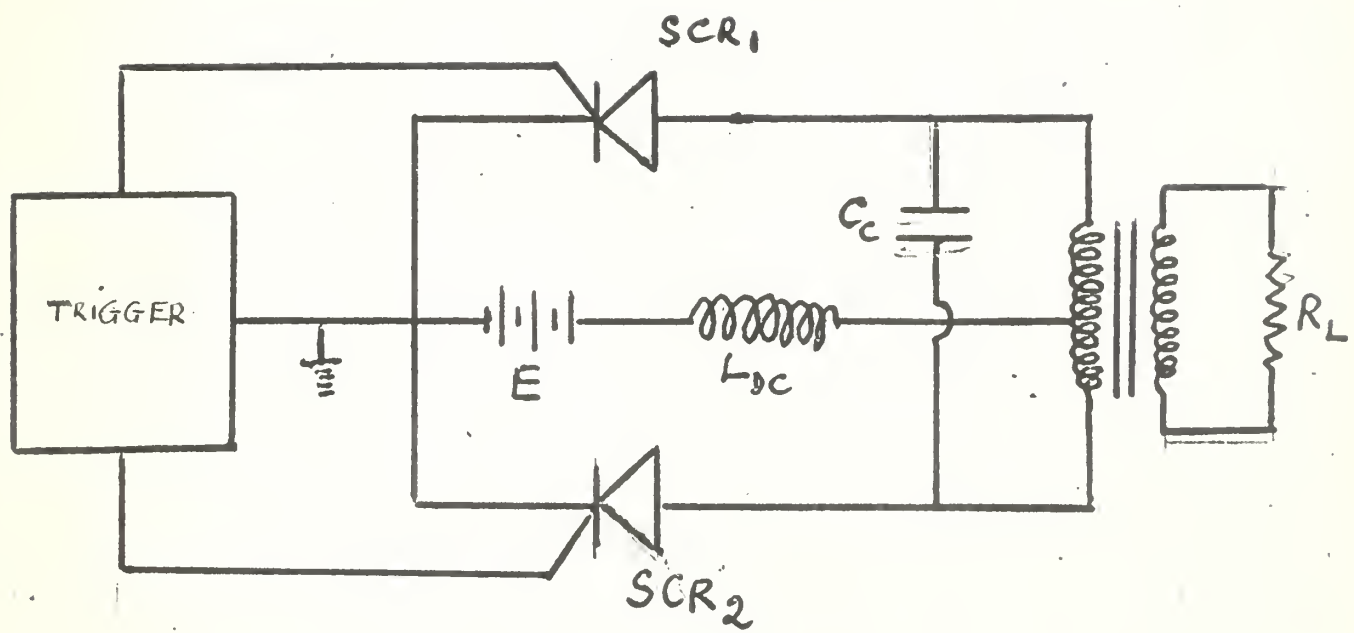
Fig. 3-1 Basic parallel inverter circuit

Fig 3-2. Trigger circuit.

Resistors	Capacitors
$R_1 = 4.7$ kΩ	C_1, $C_2 = 0.2$ μF for 3.85 KCS
$R_2 = 2.5$ kΩ (kept fixed)	C_1, $C_2 = 1.2$ μF for 540 cps
R_3, $R_4 = 330$ Ω	C_1, $C_2 = 11.2$ μF for 295 cps
R_5, $R_6 = 220$ Ω	C_3, $C_4 = 0.1$ μF
R_7, $R_8 = 2.2$ Ω	

$V = 22.5$ volt

T_1, T_2 are 2N1310 transistors

D_1, D_2 are 1N1086 diodes

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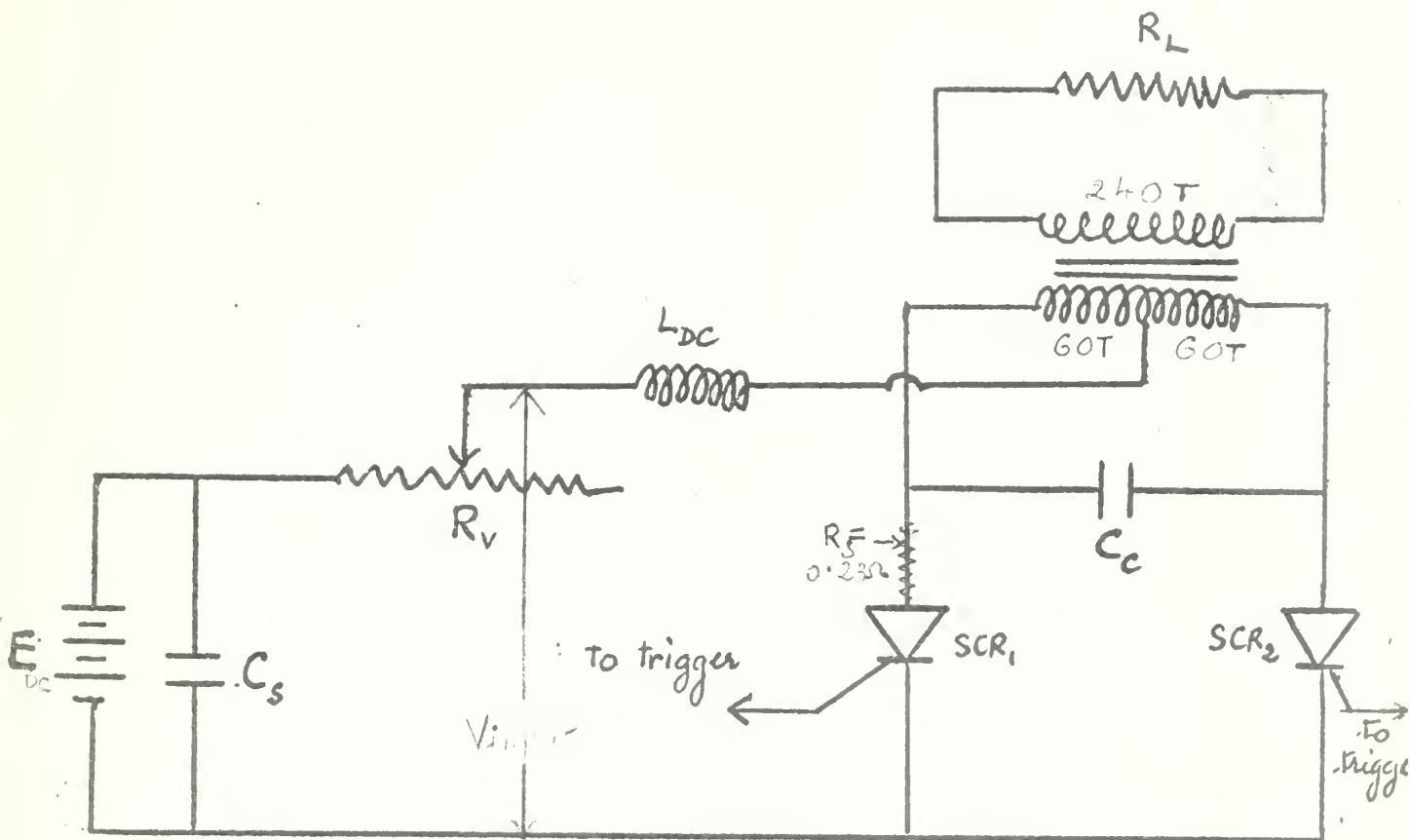
Fig. 2-3 Inverter Circuit

$E_{DC} = 30V$

$C_S = 100 F$

$C_c = 2.5 \mu F$ (can be varied)

$L_{DC} = 50 \mu H$

SCR_1, SCR_2 are the G.E. C11

Transformer is a GE 9T9341337

Primary 60 turns each half winding

Secondary 240 turns.

$R_L = 52$ (can be varied)

$R_v =$ " variac
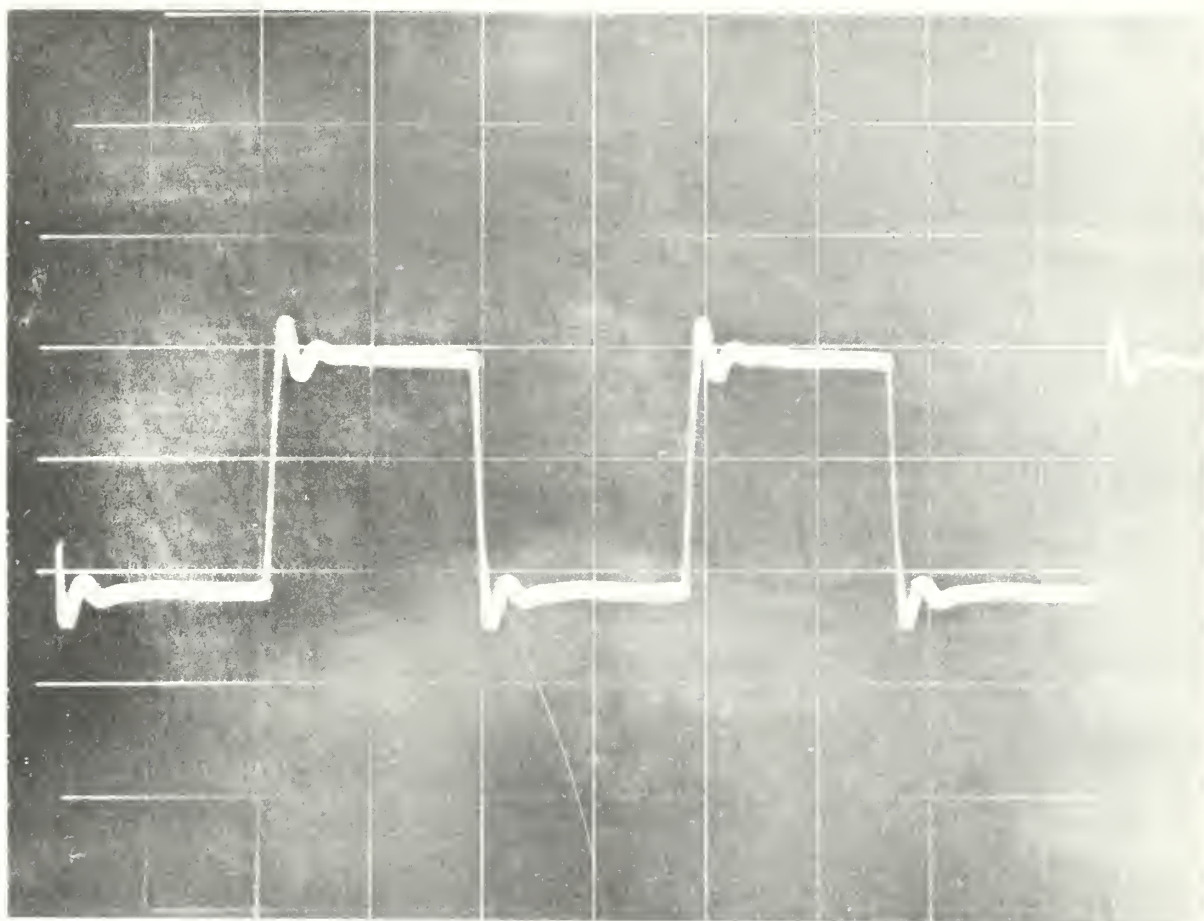
Fig. 3-5 Load voltage waveform at normal frequency.

Vertical scale   60V/enlarged cm

Horizontal scale   .5 millisecond/enlarged cm

$$\frac{T_c}{T_L} = 2.08$$

Frequency = 540 cps

V_{input} = 13 volts
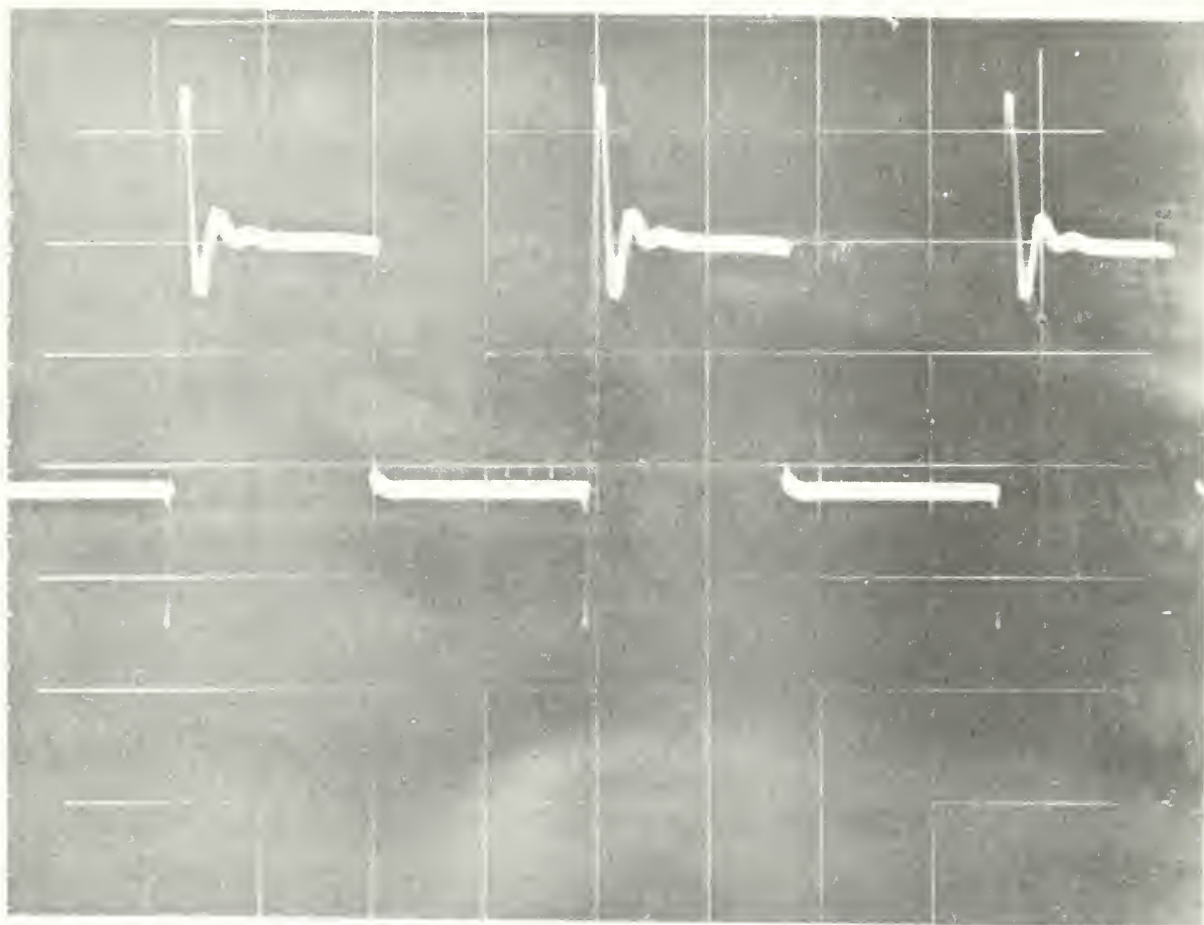
Fig. 3-6 SCR's voltage waveform

Vertical scale = 15V/enlarged cm

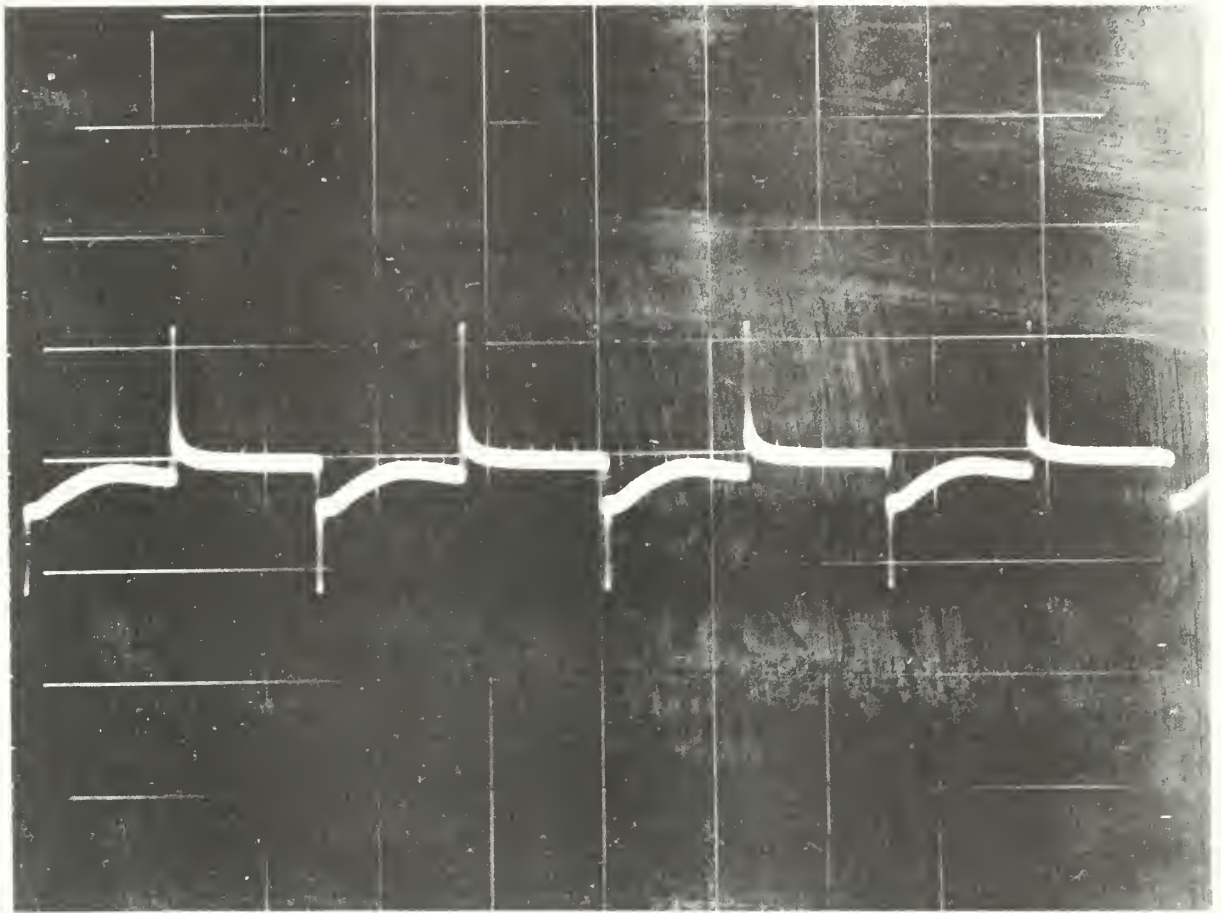Other data are the same as for Fig. 3-5.
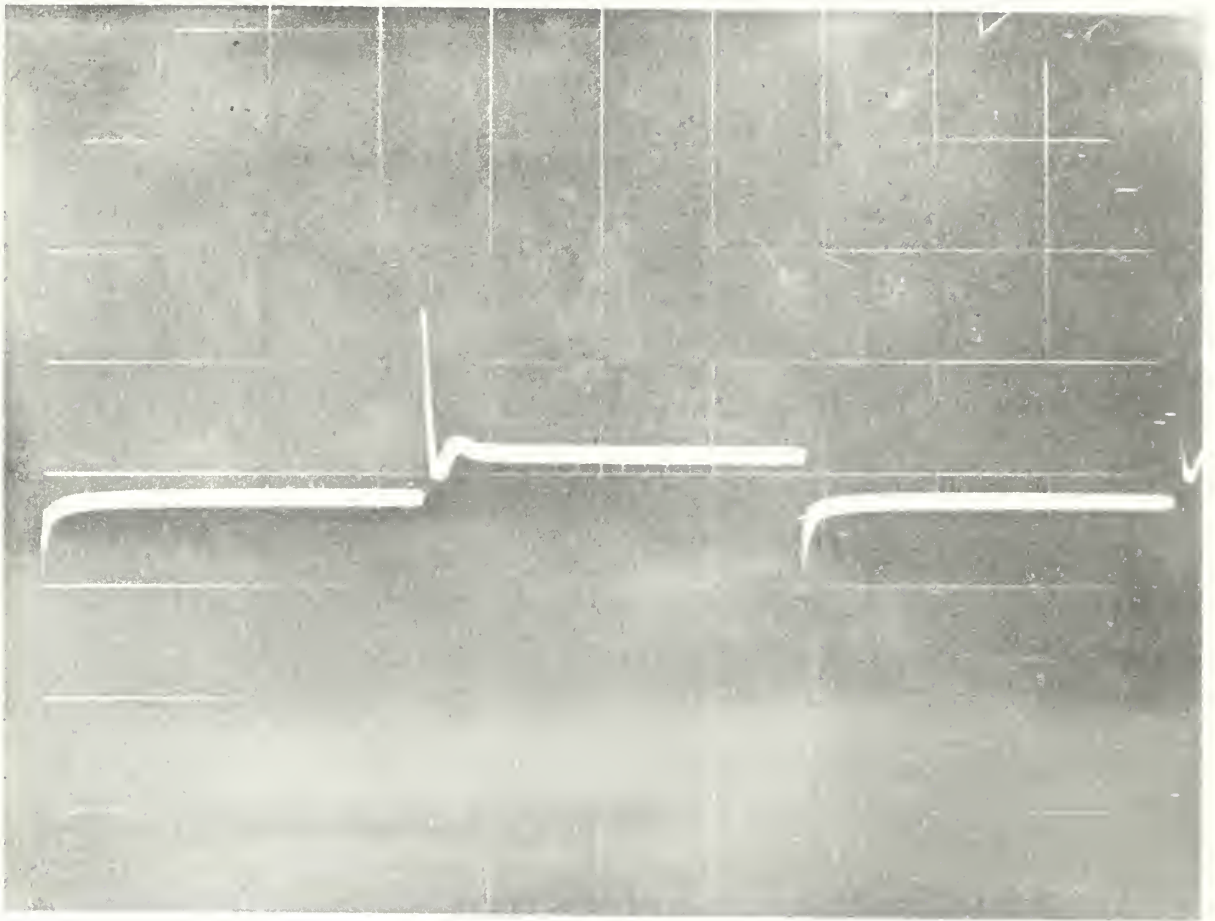
Fig. 3-7 SCR's current waveform

Vertical scale 3V/enlarged cm

Hortizontal scale .3 millisecond/enlarged cm
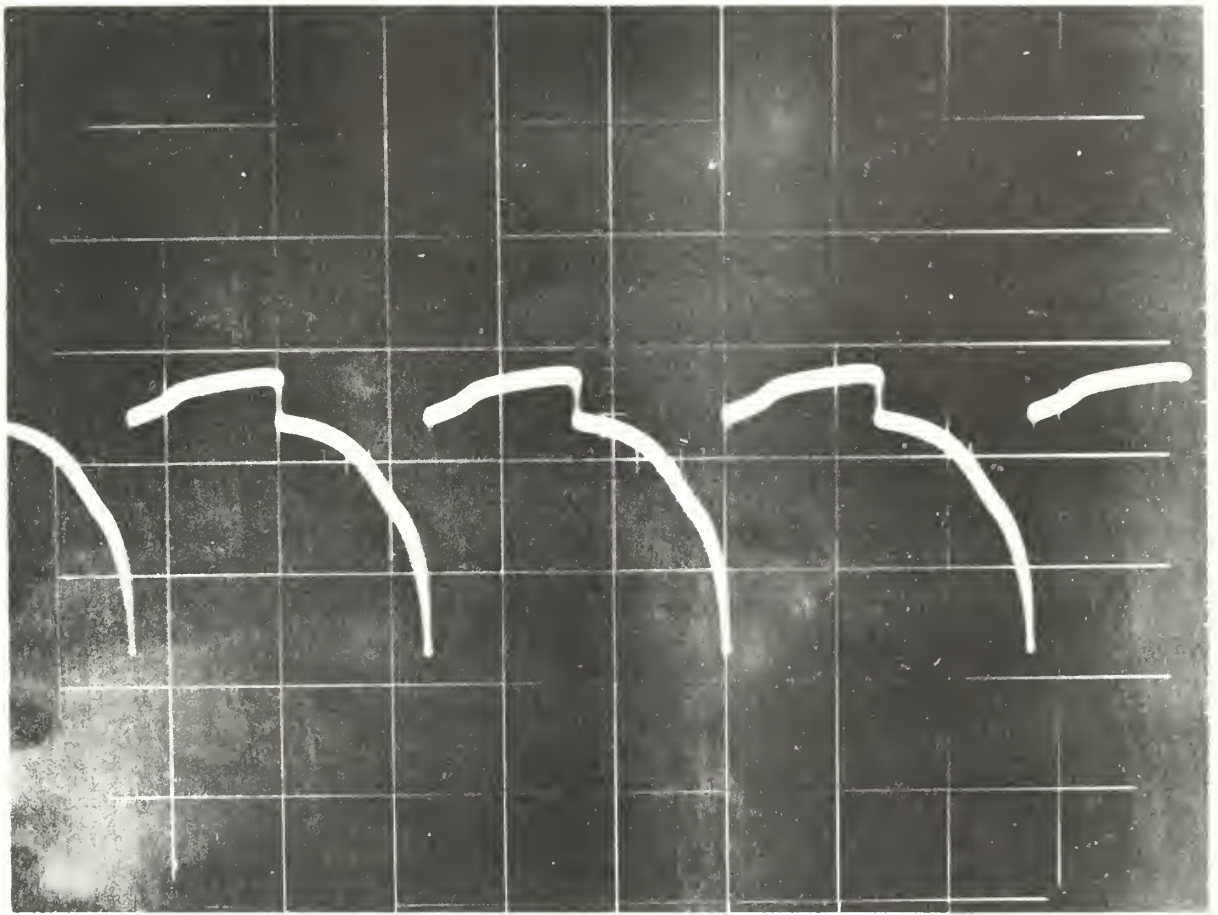
Other data are the same as for Fig. 3-5.

Fig. 3-8 Trigger voltage waveform

Vertical scale 1V/enlarged cm

Hortizontal scale 1 millisecond/enlarged cm

V = 22.5 volts (See Fig. 3-7)

Frequency 540 cps
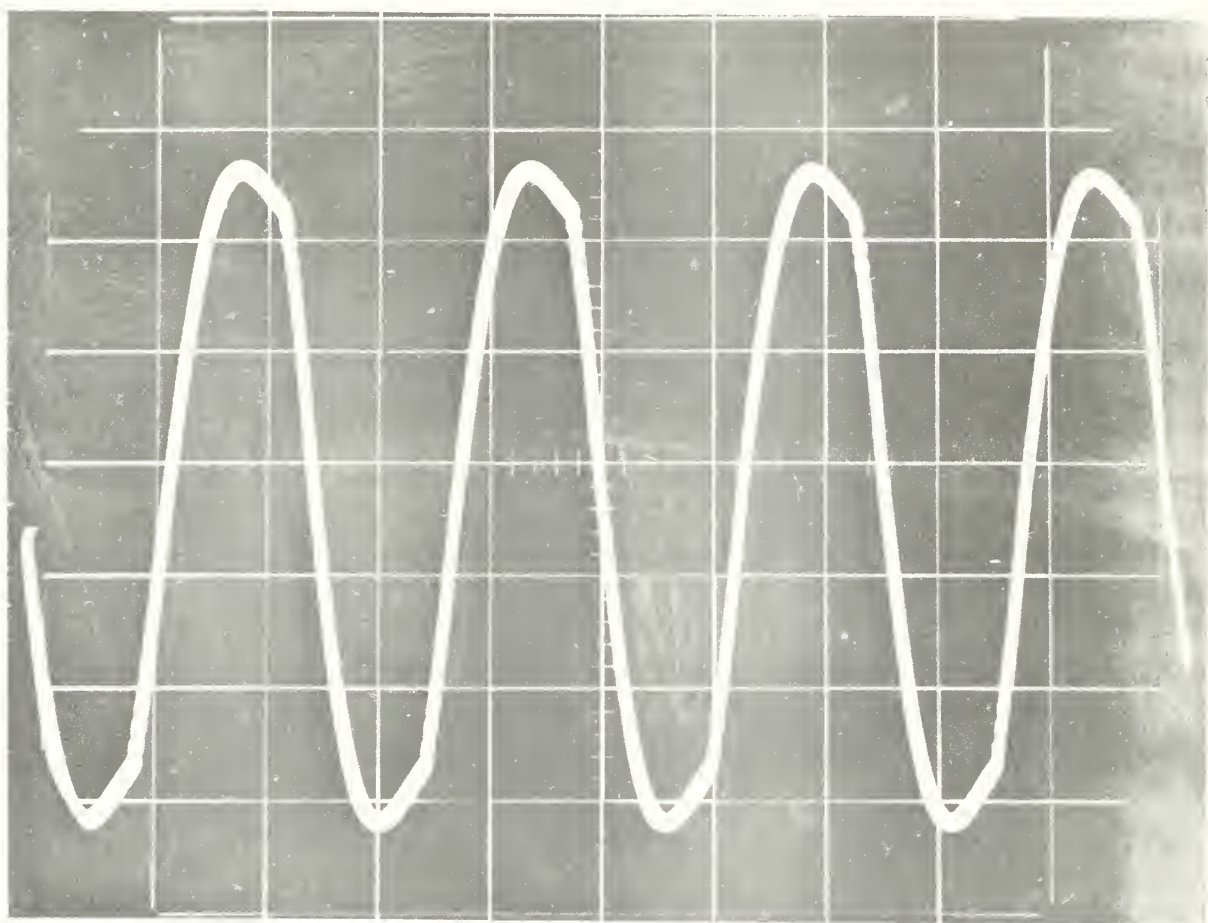
Fig. 3-9 Load voltage waveform at high frequency

Vertical scale 20V/enlarged cm

Hortizontal scale 100 μsec enlarged cm

$$\frac{T_c}{T_L} = 2.08$$

frequency = 3.85 KCS (cycles/sec)

Vinput = 14.8 volts
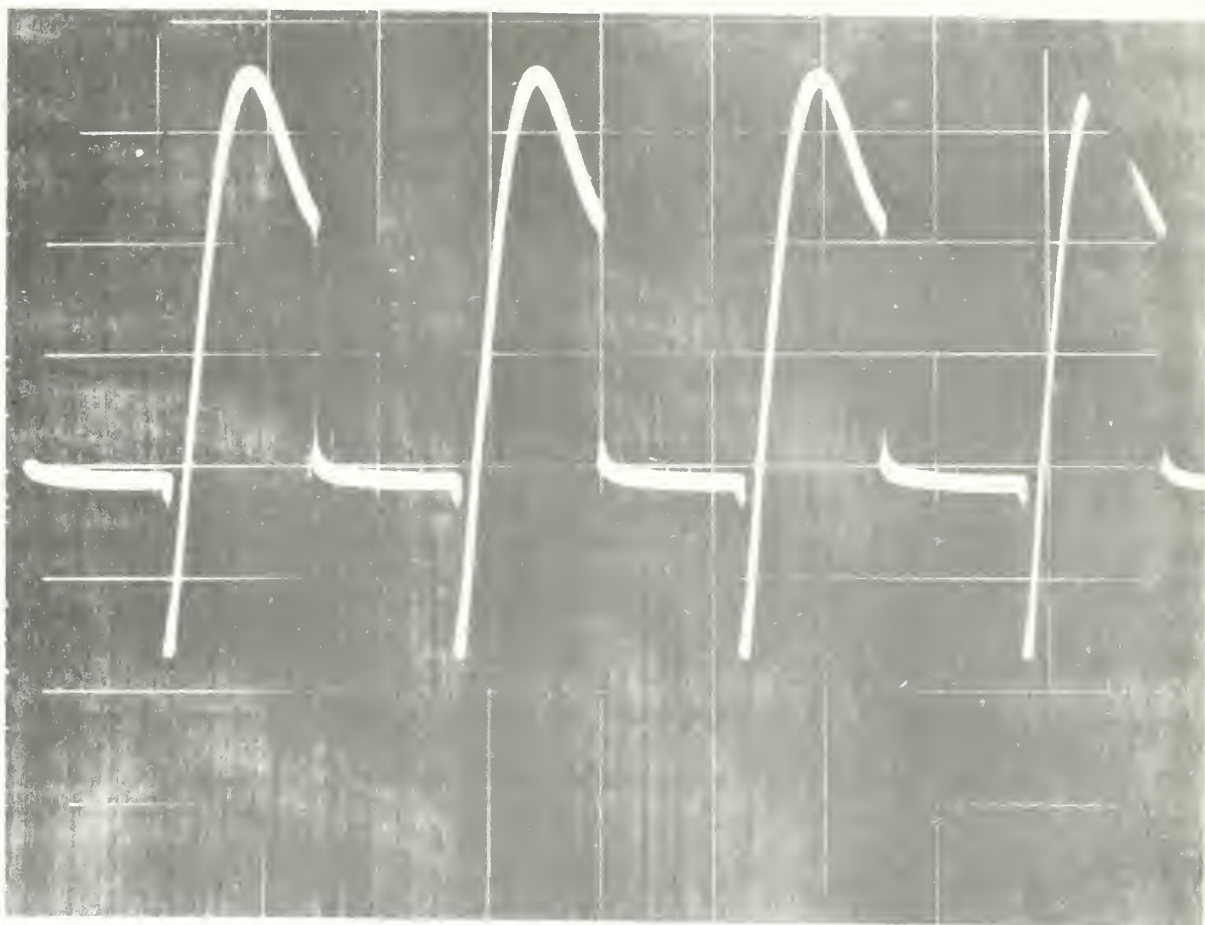
Fig. 1-10 CR's voltage waveform

Vertical scale = 10V/enlarged cm

Hoitizontal scale = 100 μsec/enlarged cm

other data are the same as for Fig. 3-9

Fig. 3-11 SCR's current waveform

Vertical scale = 10V/enlarged cm

Hortizontal scale = 100 sec/enlarged cm

Other data are the same as for Fig. 3-9

Fig. 3-12 Trigger voltage waveform

        Vertical scale = 1V/enlarged cm

        Hortizontal scale = 100 sec/enlarged cm

        V = 22.5 volts (See Fig. 3-2)

        Frequency = 3.85 KCS
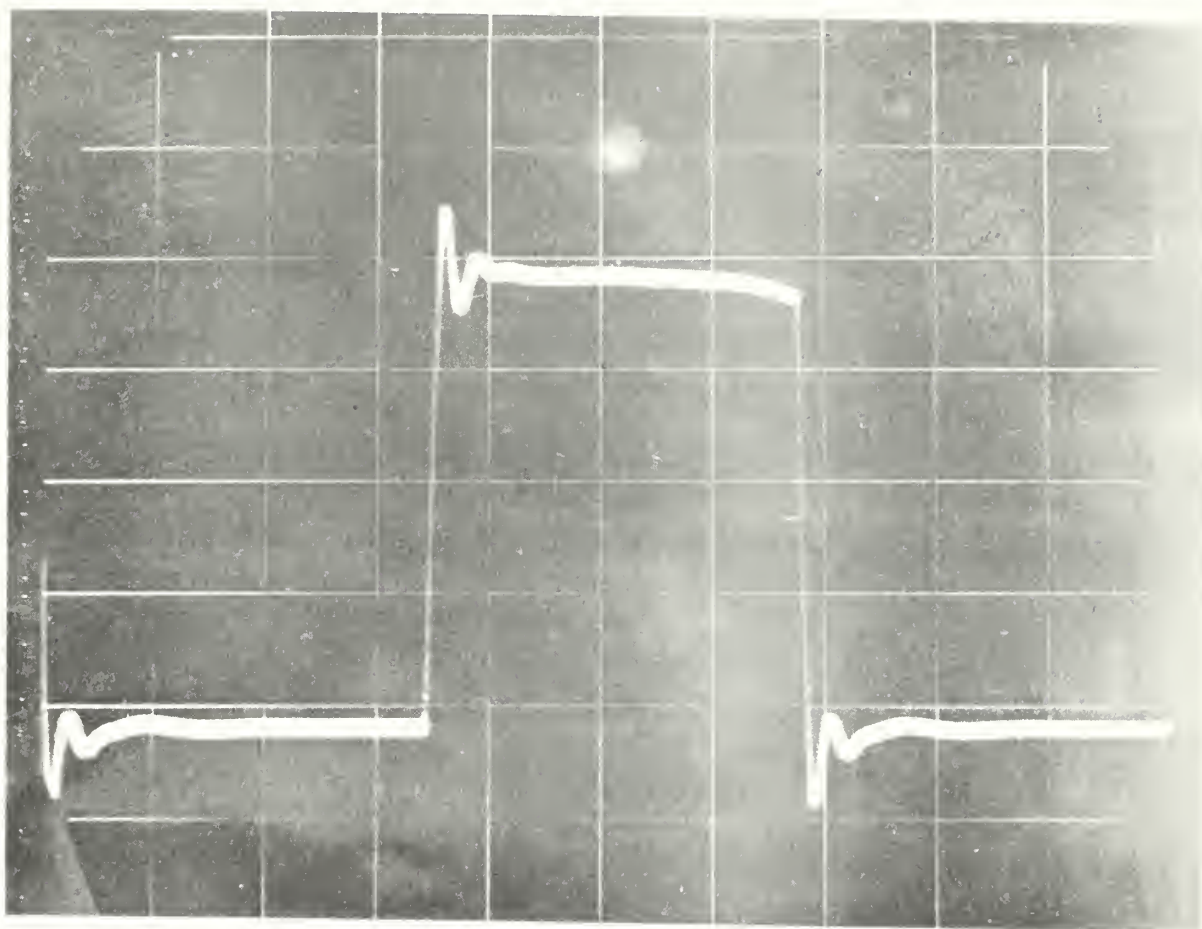
Fig. 3-13 Load voltage waveform at low frequency

Vertical scale = 30V/enlarged cm

Hortizontal scale = .5 millisecond/enlarged cm

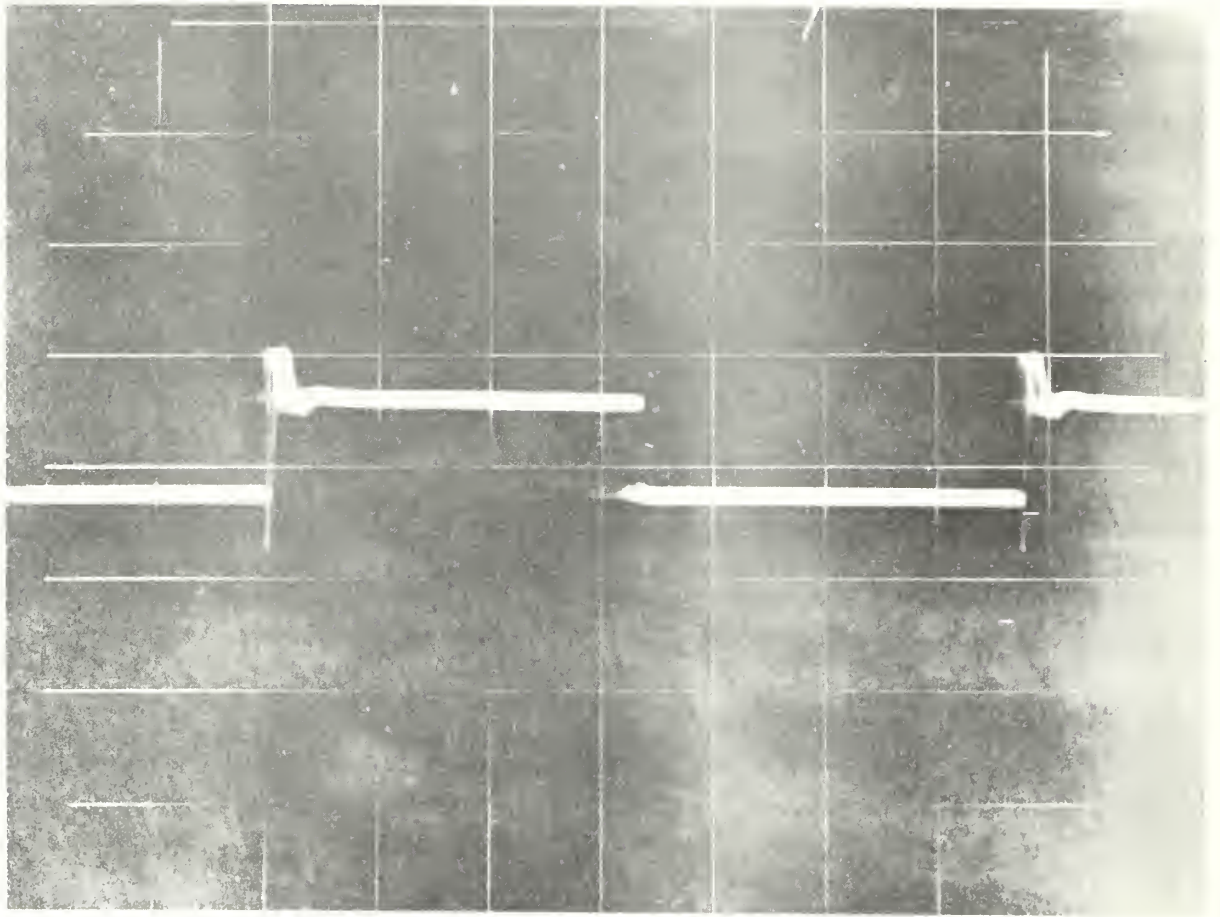$$\frac{T_c}{T_L} = 2.08$$

Frequency 295 cps

Vinput = 17.5 volts

Fig. 3-14   SCR's voltage waveform

Data are the same as for Fig. 3-13

Fig. 3-15 SCR's current waveform

Vertical scale = 1V/enlarged cm

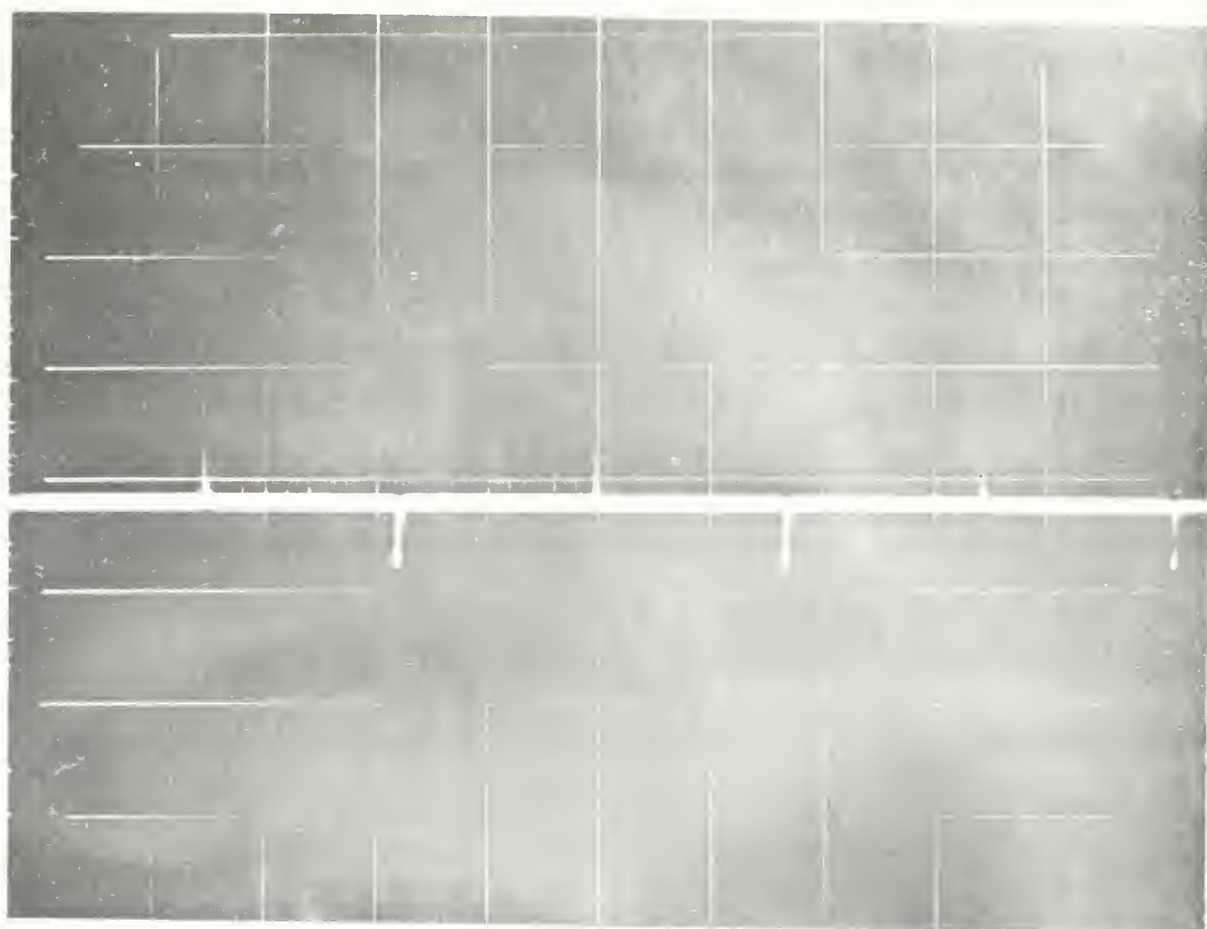All other data are the same as for Fig. 3-13

Fig. 3-16 Trigger voltage waveform

Vertical scale = 1V/enlarged cm

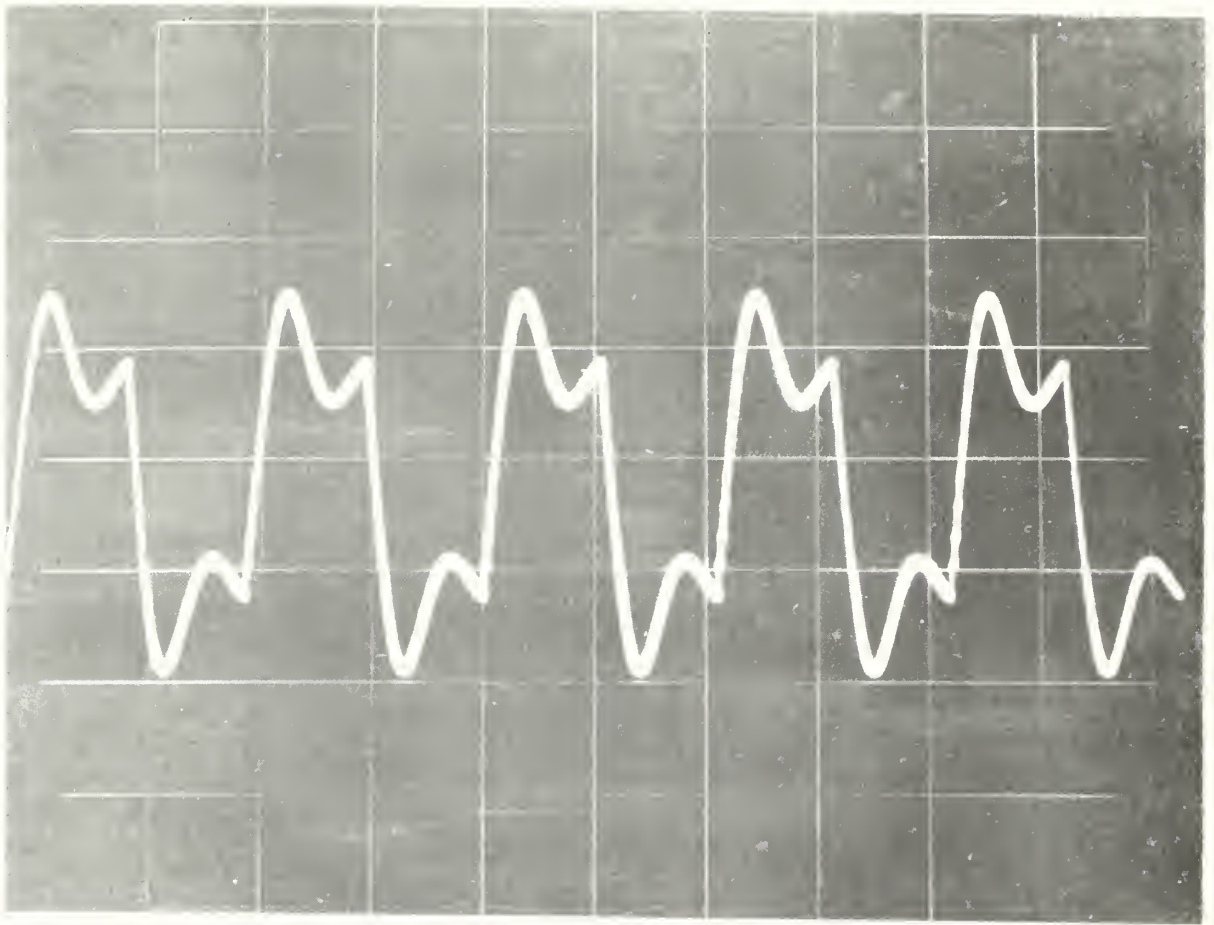Hortizontal scale = 1 millisecond/enlarged cm

Frequency = 295 cps

Fig. 3-17 Load voltage waveform at $\dfrac{T_c}{T_L}$ = 3.4

Vertical scale = $\dfrac{60V}{\text{enlarged cm}}$

Hortizontal scale = 100 μsec/enlarged cm

Frequency = 4.65 KCS
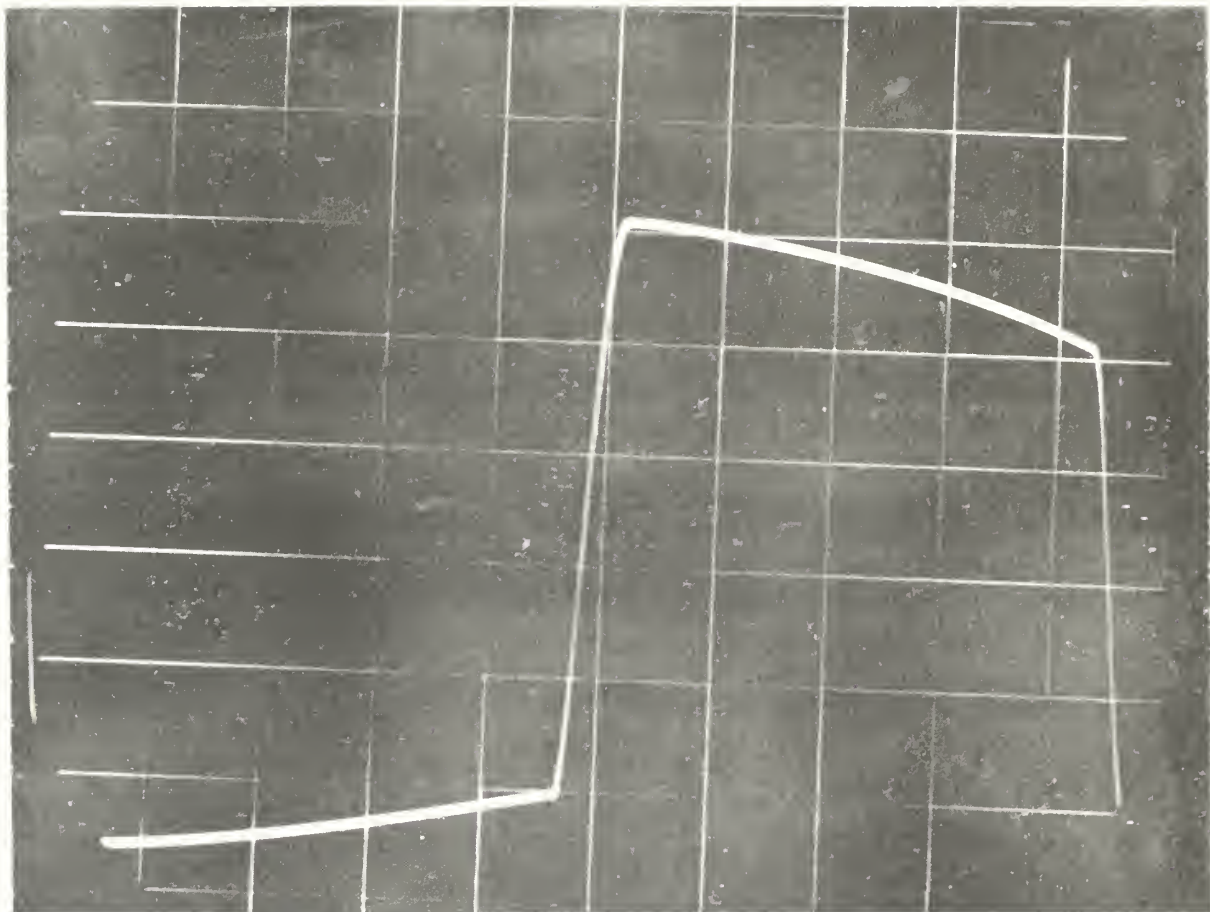
Vinput = 65 volts

Fig. 3-18 Load voltage at $\dfrac{T_c}{T_L} = 0$

Vertical scale = 58V/enlarged cm

Hortizontal scale = 200 μsec/enlarged cm

Frequency = 555 cps

Vinput = 28 Volts

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